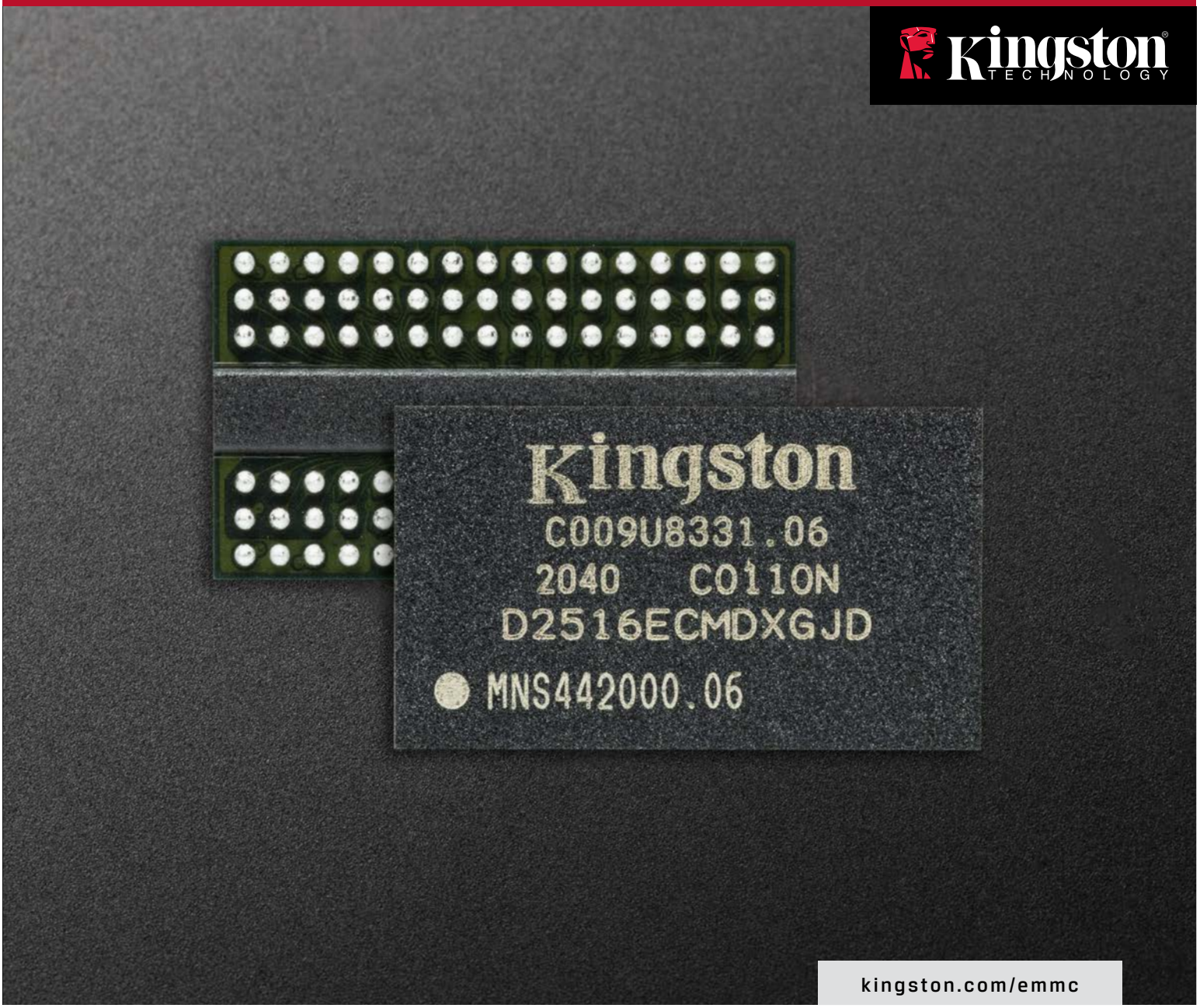

i-Temp DRAM

Kingston I-Temp DDR3/3L DRAM for embedded applications

Kingston on-board DRAM is designed to meet the needs of embedded applications and offers a low-voltage option for lower power consumption.

MARKET SEGMENTS

Industrial IoT / robotics & factory automation

5G networking/telecommunications communication modules (Wi-Fi routers and mesh devices)

Wearables (smart watches, health monitors, AR & VR)

Smart home (sound bars, thermostats, fitness equipment, vacuums, beds, taps)

Smart city (HVAC, lighting, power monitoring/ metering, parking meters)

i-Temp DDR3/3L PART NUMBERS AND SPECIFICATIONS

Part number	Capacity	Description	Package	Configuration (words x bits)	Speed Mbps	VDD, VDDQ	Operating temperature
D1216ECMDXGJDI	2Gb	96 ball FBGA DDR3/3L	7.5x13.5x1.2	128Mx16	1866 Mbps	1.35V	-40°C ~ +95°C
D2568ECMDPGJDI	2Gb	78 ball FBGA DDR3/3L	7.5x10.6x1.2	256Mx8	1866 Mbps	1.35V	-40°C ~ +95°C
D2516ECMDXGJDI	4Gb	96 ball FBGA DDR3/3L	7.5x13.5x1.2	256Mx16	1866 Mbps	1.35V*	-40°C ~ +95°C
D5128ECMDPGJDI	4Gb	78 ball FBGA DDR3/3L	7.5x10.6x1.2	512Mx8	1866 Mbps	1.35V*	-40°C ~ +95°C
D2516ECMDXGMEI	4Gb	96 ball FBGA DDR3/3L i-Temp	7.5x13.5x1.2	256Mx16	2133 Mbps	1.35V*	-40°C ~ +95°C
B5116ECMDXGJDI	8Gb	96 ball FBGA DDR3/3L i-Temp	9x13.5x1.2	512Mx16	1866 Mbps	1.35V*	-40°C ~ +95°C

*Backward compatible to 1.5V VDD, VDDQ

KEY FEATURES

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realised by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DOS and /DQS) is transmitted/received with data for capturing data at the receiver
- DOS is edge-aligned with data for READS; centre-aligned with data for WRITES
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DOS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data Mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-die termination (ODD for better signal quality)
  - Synchronous ODT
  - Dynamic CDT
  - Asynchronous ODT
- Multi-Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DO drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- RESET pin for power-up sequence and reset function
- SRT range: normal/extended
- Programmable output driver impedance control