IEEE TOPOLOGY REVIEW OF DC/DC CONVERTERS

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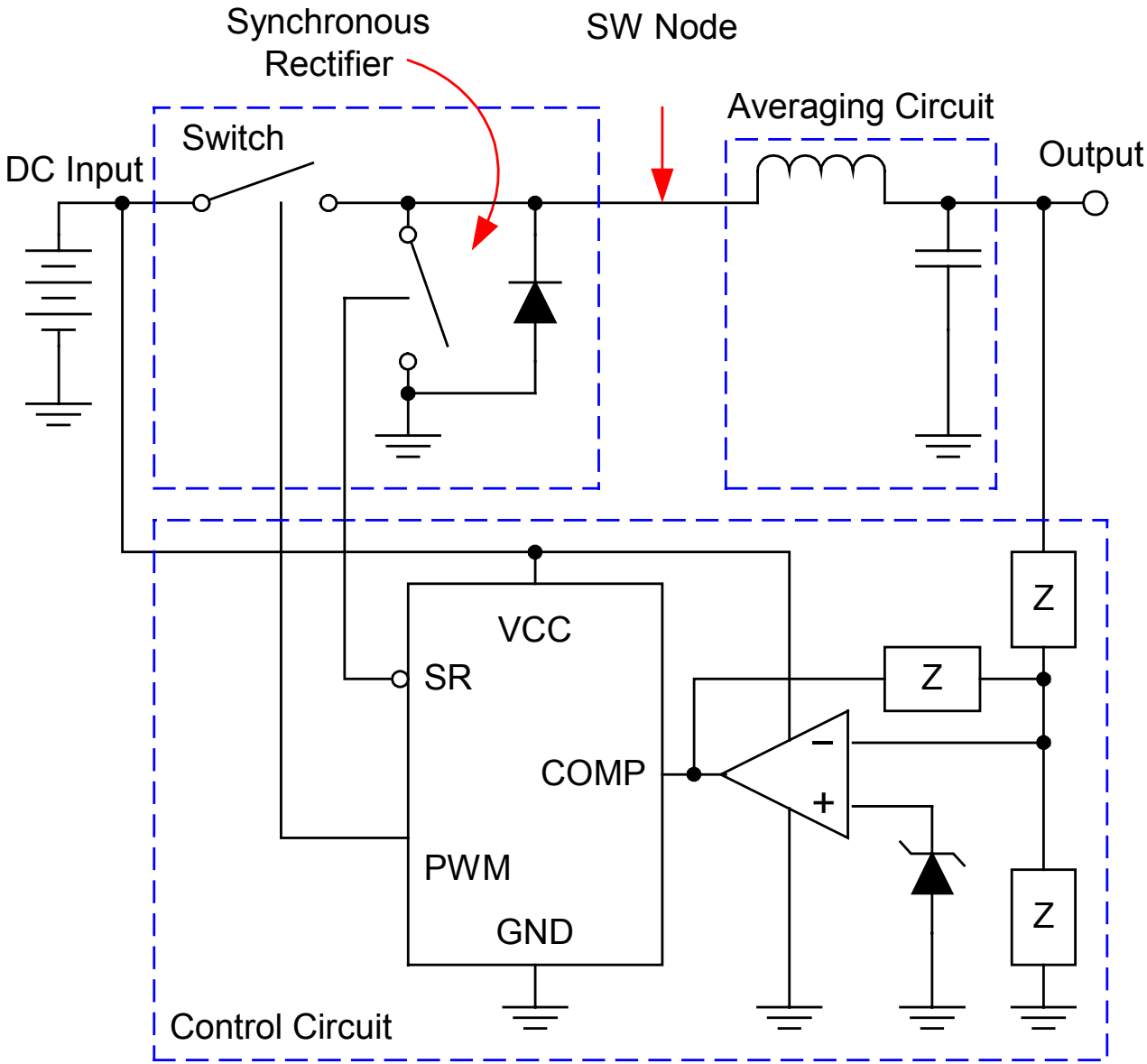
IEEE TOPOLOGY REVIEW

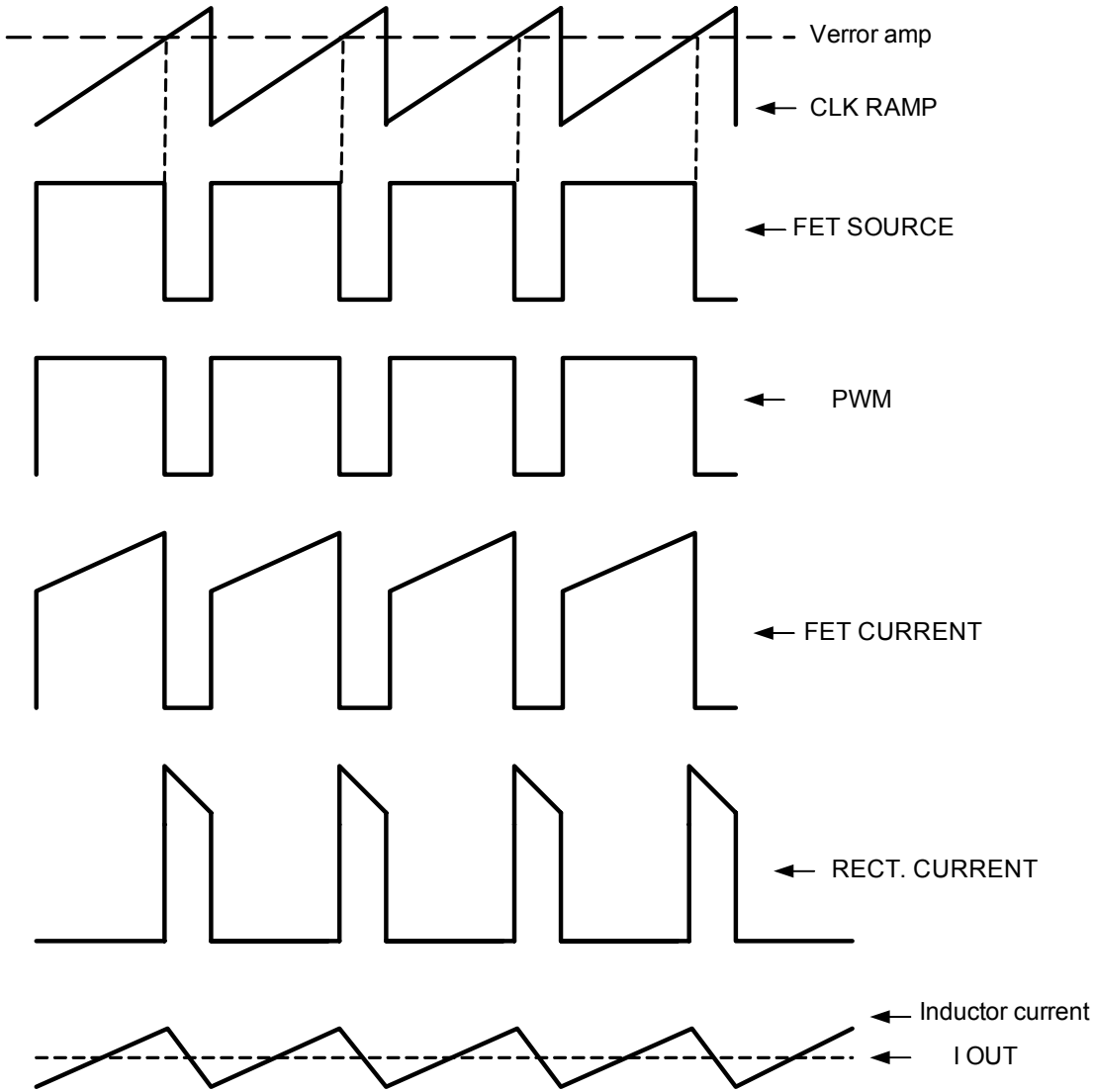
- Buck converter theory of operation
  - Discontinuous vs. Continuous mode of operation
  - Voltage mode feedback and Current mode feedback
  - Design considerations
- Boost converter theory of operation
  - Design considerations
- Flyback converter theory of operation
  - Design considerations
- SEPIC Converter theory of operation
  - Design considerations

Synchronous Buck



Synchronous Buck Waveforms

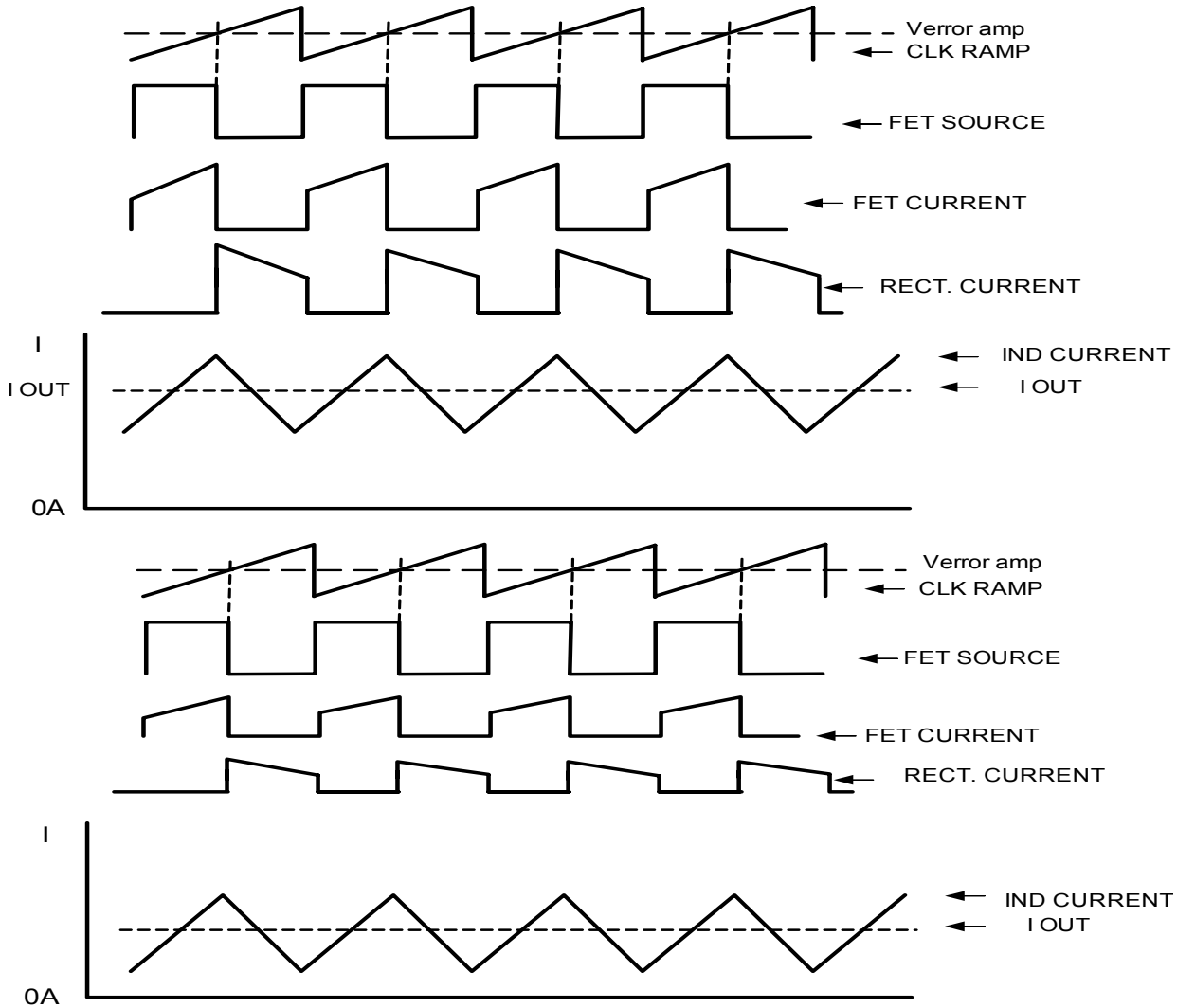
Continuous Conduction Mode



Synchronous Buck Waveforms

Continuous Conduction Mode

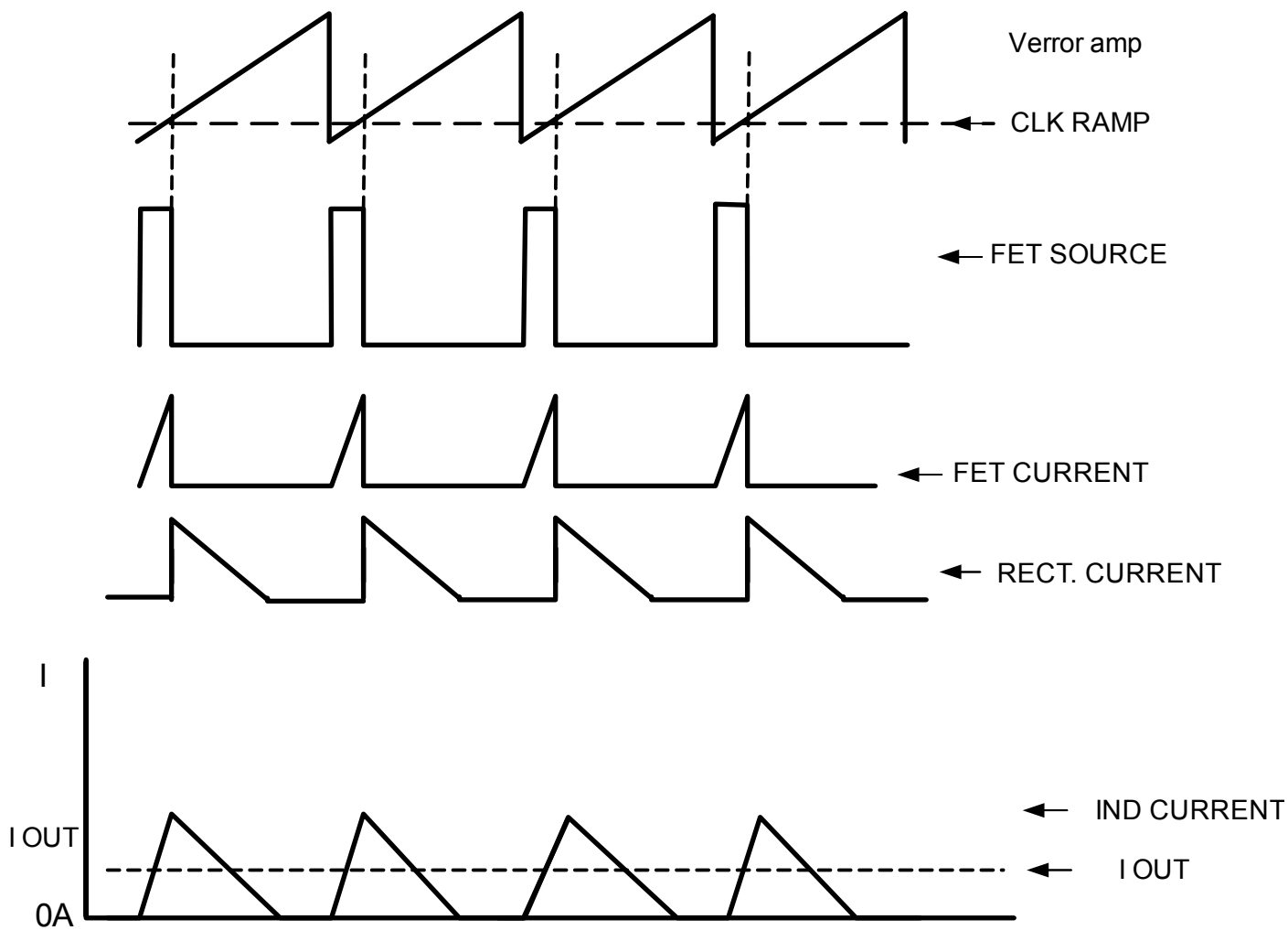
As the load current goes down the converter becomes less continuous but D is still equal to Vout /Vin



Synchronous Buck Waveforms

Discontinuous Conduction Mode

The load current has gone down the the point where the converter becomes discontinuous D no longer equals Vout /Vin



Basic Relationships

Continuous Conduction Mode (CCM)

$$D = \frac{t_{on}}{Ts} = \frac{V_{out}}{V_{in}}$$

$$\Delta I_{out} = \frac{(V_{in} - V_{out}) \cdot D \cdot Ts}{L}$$

Discontinuous Conduction Mode (DCM)

$$D = \sqrt{\frac{2L \cdot I_O}{Ts} \cdot \frac{V_{out}}{V_{in}^{\,2} - V_{in} \cdot V_{out}}}$$

Inductor Considerations

- Benefits of low L values
  - Lower DCR
  - Higher Isat
  - Higher di/dt
    - Transient response improves
    - Less output capacitance required for given transient performance

$$B := \frac{Vrms \cdot 10^{8}}{4.44 \cdot Ae \cdot N \cdot f}$$

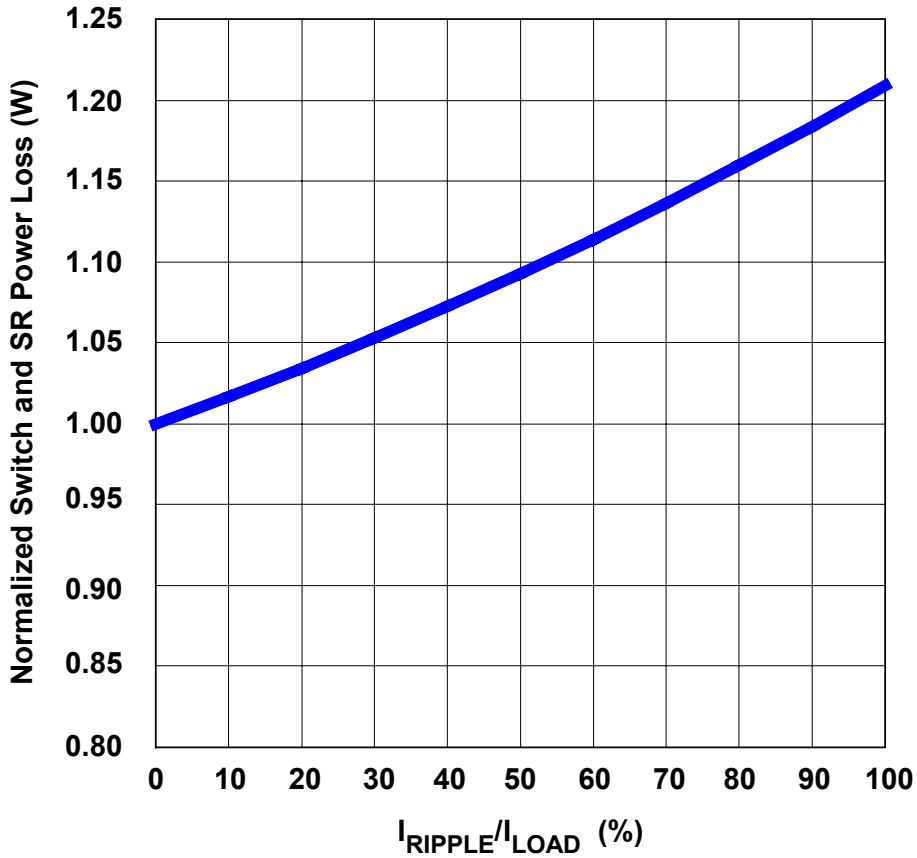
- Benefits of high L values
  - Lower ripple current
    - Lower AC losses (skin effect, hysteresis)
    - Lower RMS current in FETs
    - Lower RMS capacitor current (mainly output)
    - Continuous inductor current over broader load range
    - Less C required for equivalent output ripple

General Inductor Guidelines

- Size for ΔI_L to be 10% to 30% of full load current
- Winding losses usually dominate

$$PL_{AVG} = IL_{RMS}^{\ 2} \cdot RL \quad \text{where} \quad IL_{RMS}^{\ 2} = \sqrt{I_{out}^{\ 2} + \frac{\Delta IL_{pp}^{\ 2}}{12}}$$

Inductor and FETs



- Increasing ripple increases losses
- Similar effect for capacitor ESR loss

MOSFETs

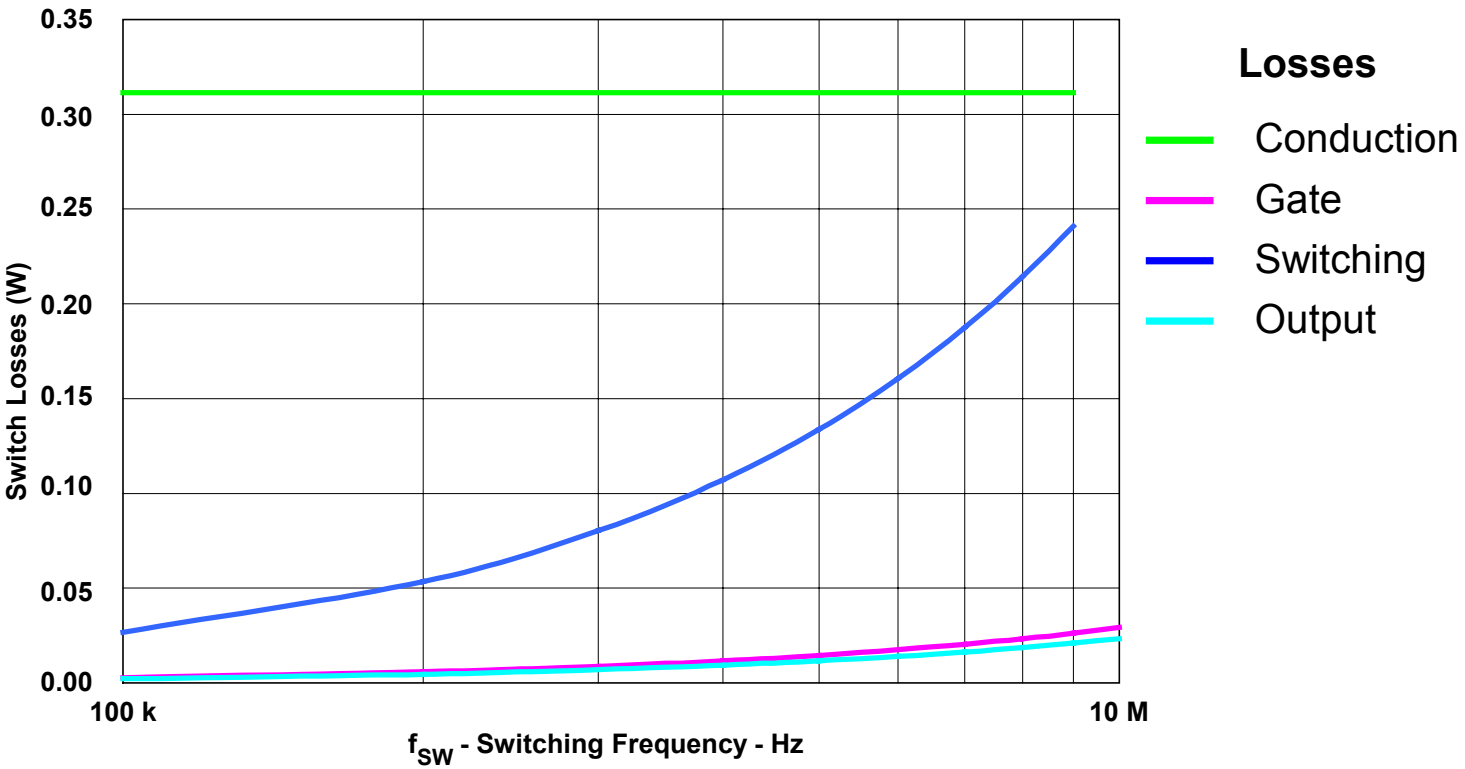
- Both main switch and synchronous rectifier should be N-type for best efficiency

- Many interrelated issues
  - Output capacitance vs. switching loss
  - Gate capacitance vs. switching speed
  - Gate capacitance vs. driver power loss

- Primary Tradeoffs
  - Package
  - Power loss
  - Cost

Switch FET

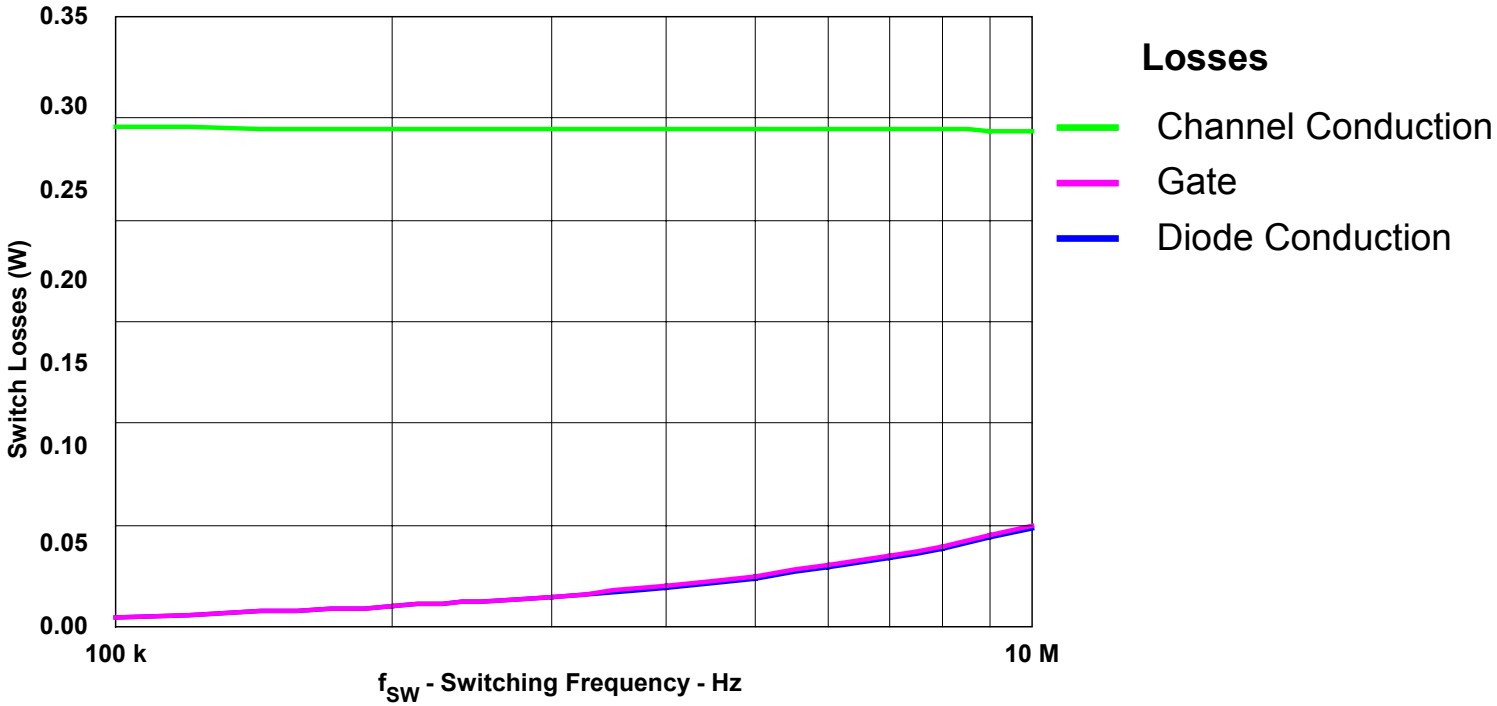
Losses vs. Frequency



- Data for Si4866DY switch, Si4836DY rectifier, 2A ripple current and 10A load

Rectifier FET

Losses vs. Frequency

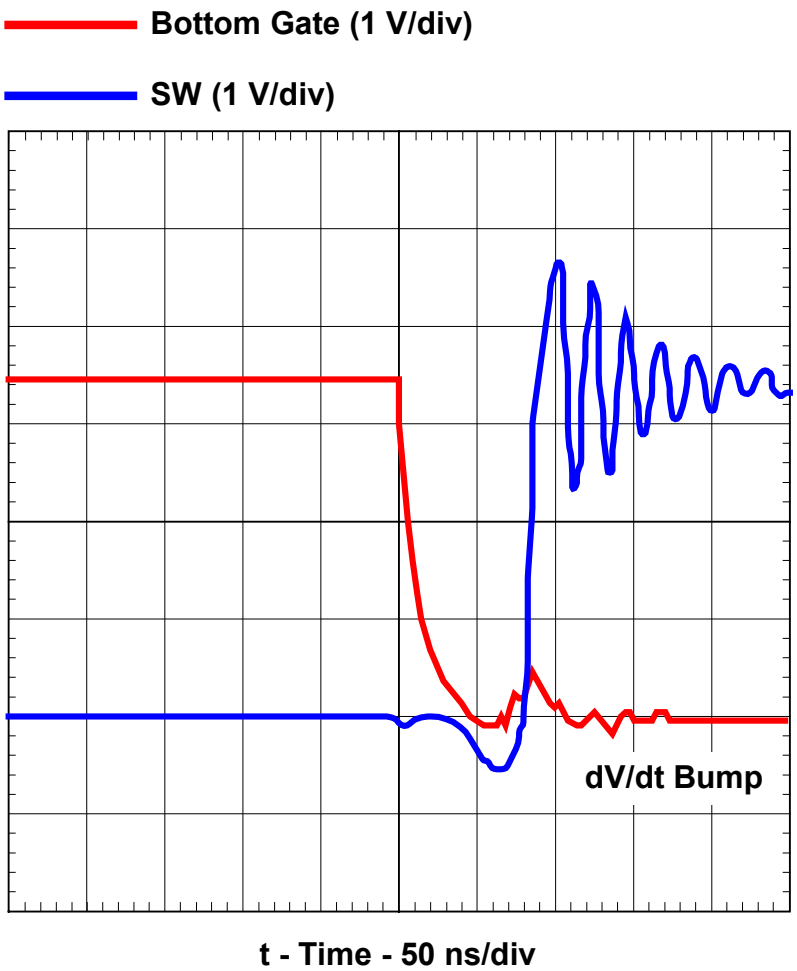


- Note rise in diode conduction loss as Fs rises.
- Data assumes 20-ns of diode conduction time per SW edge

FET Selection

- Compare different FETs in both positions
- In general higher F and higher input voltage mean Higher switching losses therefore use lower Qg switch FET to cut switching losses
- For rectifier FET, low $R_{DS(on)}$ is most important, but don't ignore gate power

SW Node Ringing



- Can affect converter operation
- Worst on rising edge of SW (highest di/dt transition)
- Caused by parasitic L and C
  - L in the FET from the SW node to Vin or GND
  - C from SW node to GND
  - High layout dependence

SW Node Ringing Remedies

- Improve layout
  - Minimize loop areas
  - Minimize trace inductance
  - Keep SW node area low (secondary effect, conflicts with cooling rectifier FET)
- Slow down SW node edge transitions
  - Series gate resistor in switch FET gate lead
- Add a snubber

Power Capacitors

Selection Considerations

- Power Dissipation
  - ESR
- Ripple Performance
  - ESR
- Transient Performance
  - ESR
  - Capacitance
  - ESL
- Cost
- Size
- Reliability

Relative Capacitors Characteristics

- Standard Al Electrolytic
  - High ESR
  - Low cost
  - Low current capability
  - Not really suited to DC/DC converters
- OSCON
  - Low ESR
  - Medium cost
  - High current capability

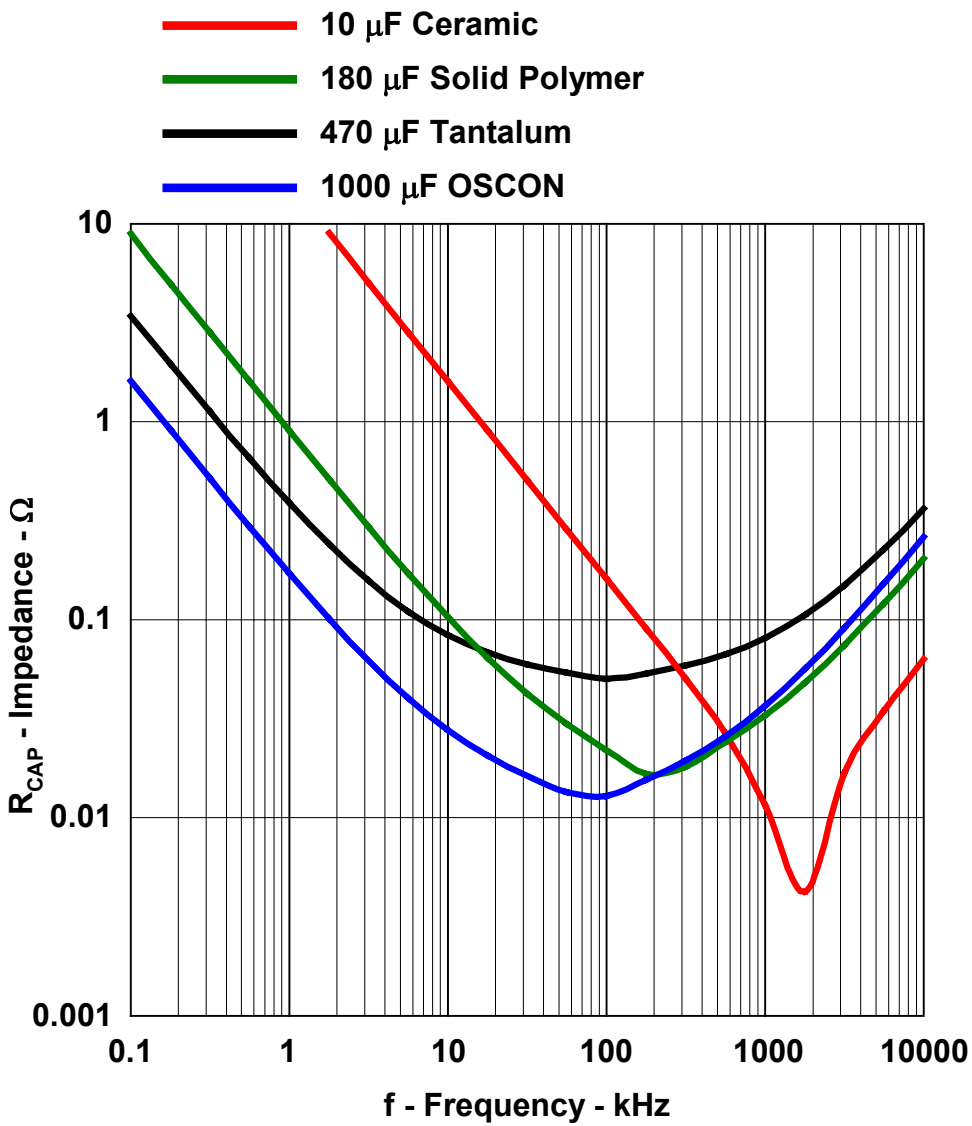
Relative Capacitors Characteristics

- Solid Polymer
  - Low ESR
  - Very high cost
  - Medium current capability
- POSCAP
  - Low ESR
  - High cost
  - Medium current capability

Relative Capacitors Characteristics

- Tantalum
  - Medium ESR
  - Medium cost
  - Medium low current capability
- Ceramic
  - Very low ESR
  - Very high cost
  - High current capability in bulk

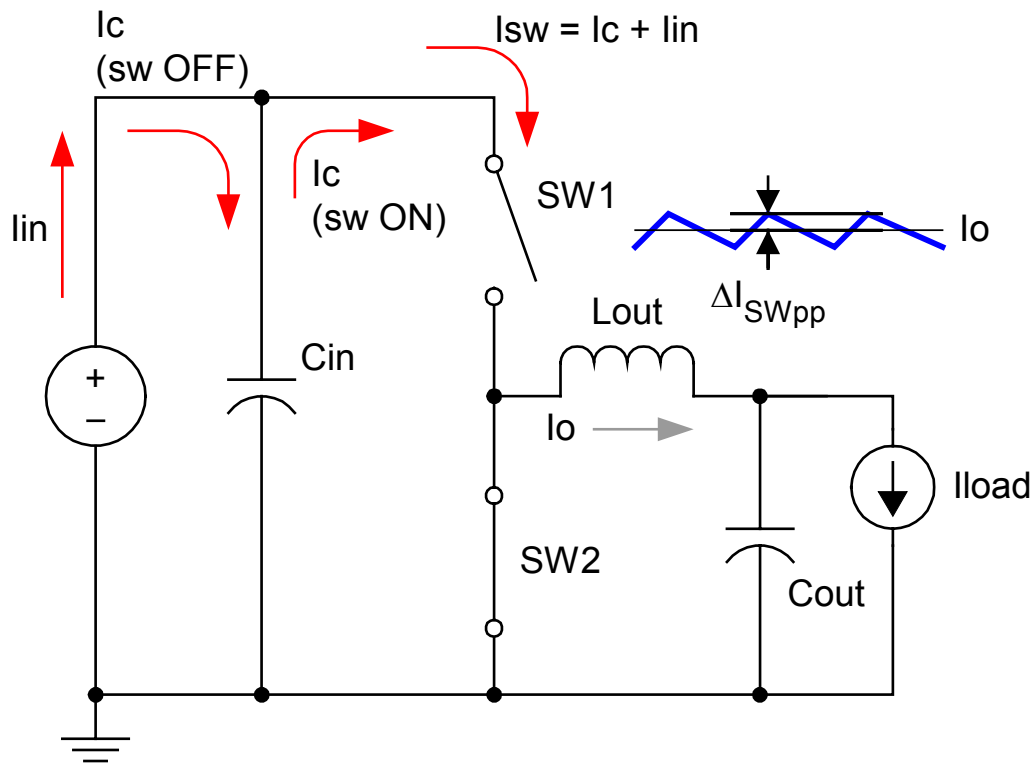
Capacitor Impedance



Choosing Capacitor Size

- Input Filter
  - Sized for AC current handling
- Output Filter
  - Transient events on load
  - Output voltage ripple

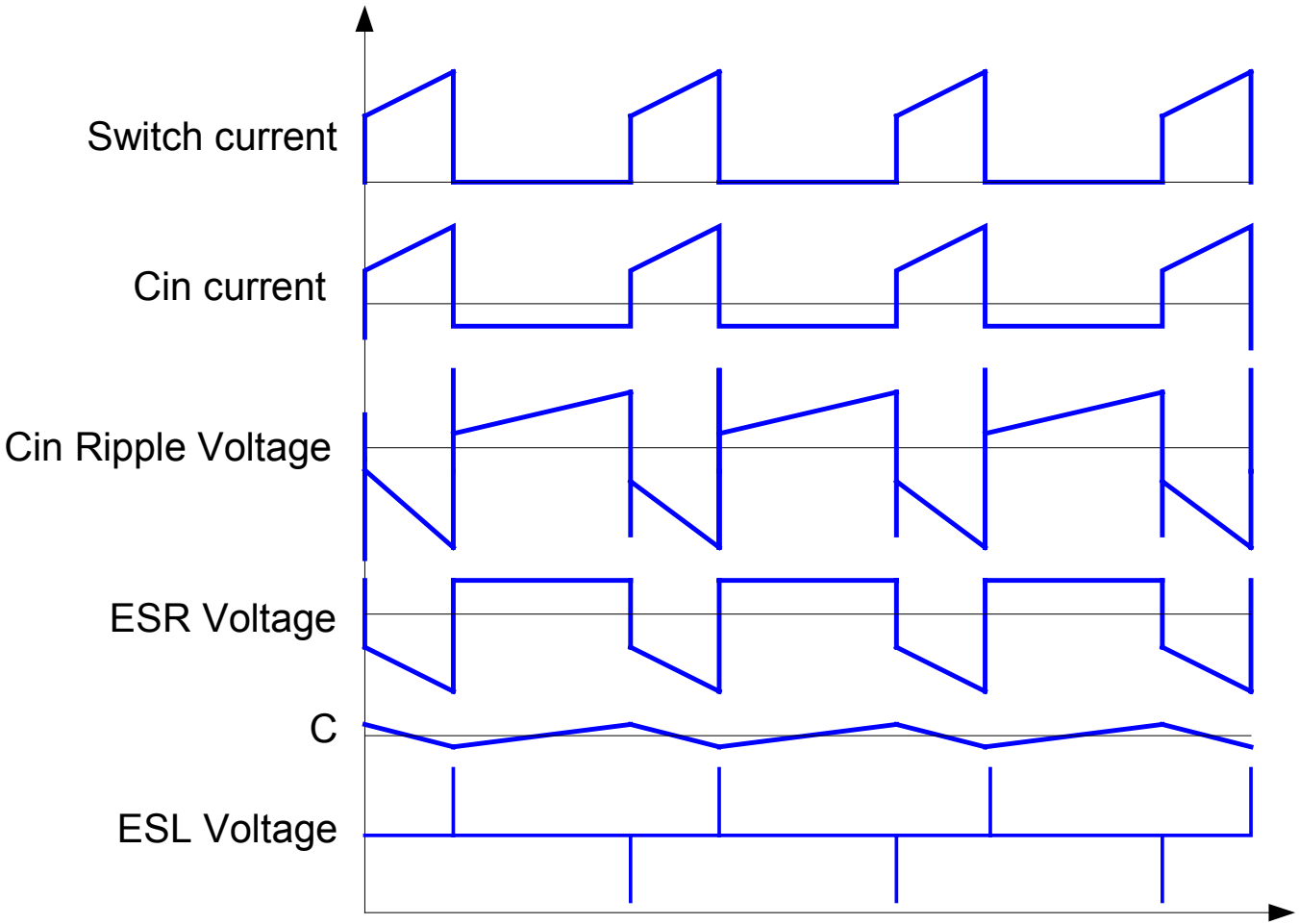
Input Capacitor Current



$$P_{cap} = I_{cap_{RMS}}{}^{2} \cdot ESR_{cap}$$

$$I_{cap_{RMS}} = \sqrt{\left[(I_{SW\,pk} - I_{in\,avg})^2 + \frac{\Delta I_{SW\,pp}{}^{2}}{12} \right] \cdot D + I_{in\,avg}{}^{2} \cdot (1 - D)}$$

Input Ripple Voltage



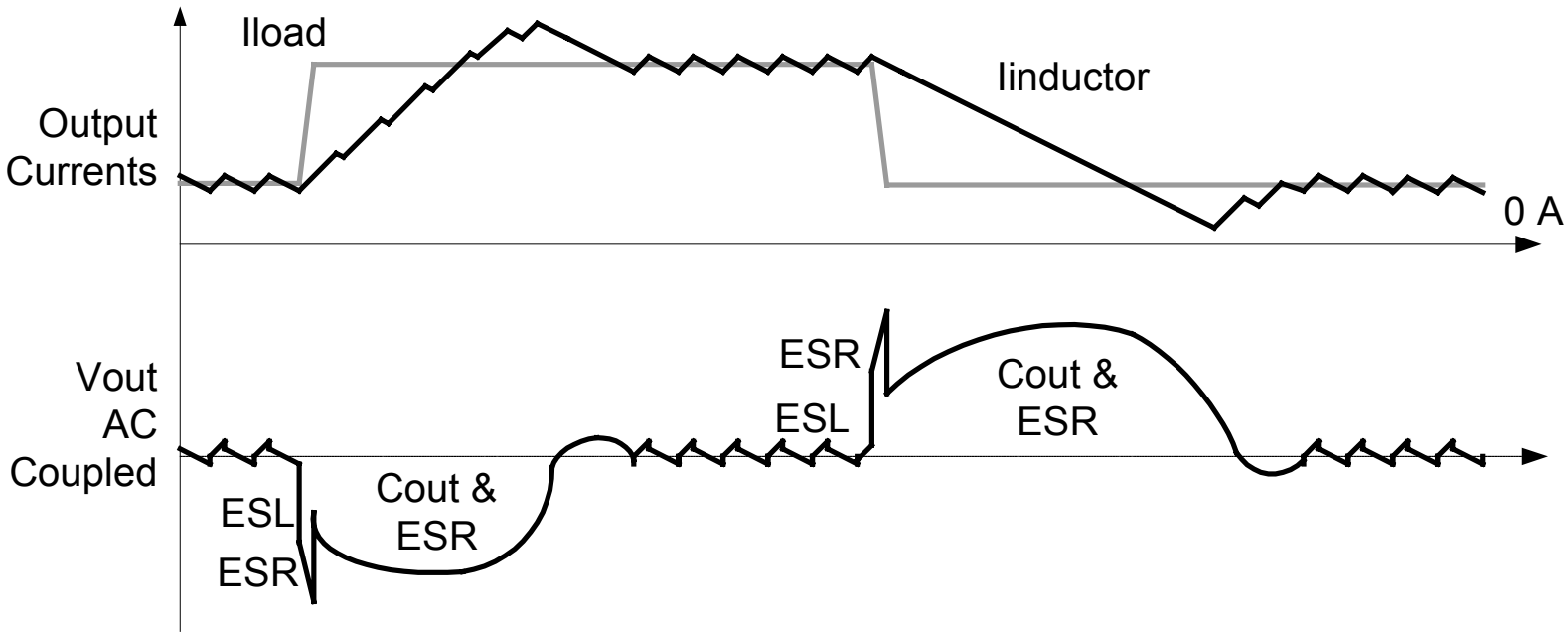
- Usually a secondary consideration
- Contribution from ESR, ESL and capacitance value

Output Capacitor Criteria

Selection Considerations

- Transient performance
  - Bulk capacitance
  - ESR
  - ESL
- Output Ripple
  - ESR
  - Bulk value
  - ESL has minor effect

Transient Performance

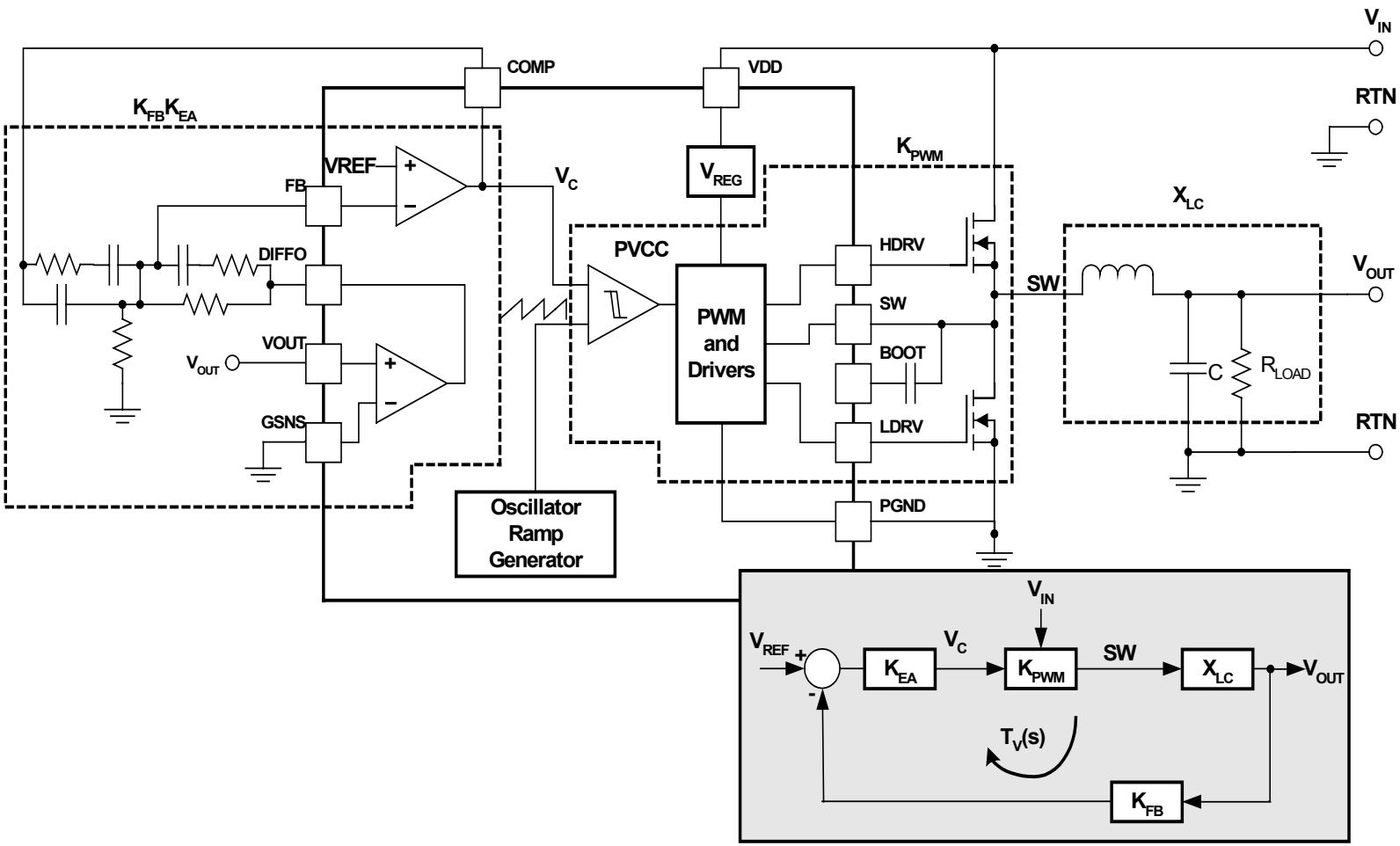


Output Capacitor

Selection Considerations

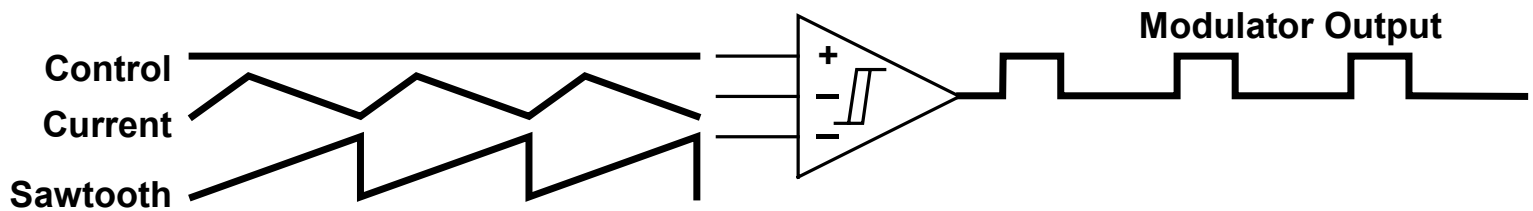
- 2A to 10A load step @ 15A/μs
- Use 470μF SP: 15mΩ, 3nH
- To help reduce spikes, add two 10μF ceramics
- Yields
  - 24.5mV undershoot
  - 39mV overshoot
  - 8mV spikes
  - 21mV of ripple

AC VMC Model for Buck Converter

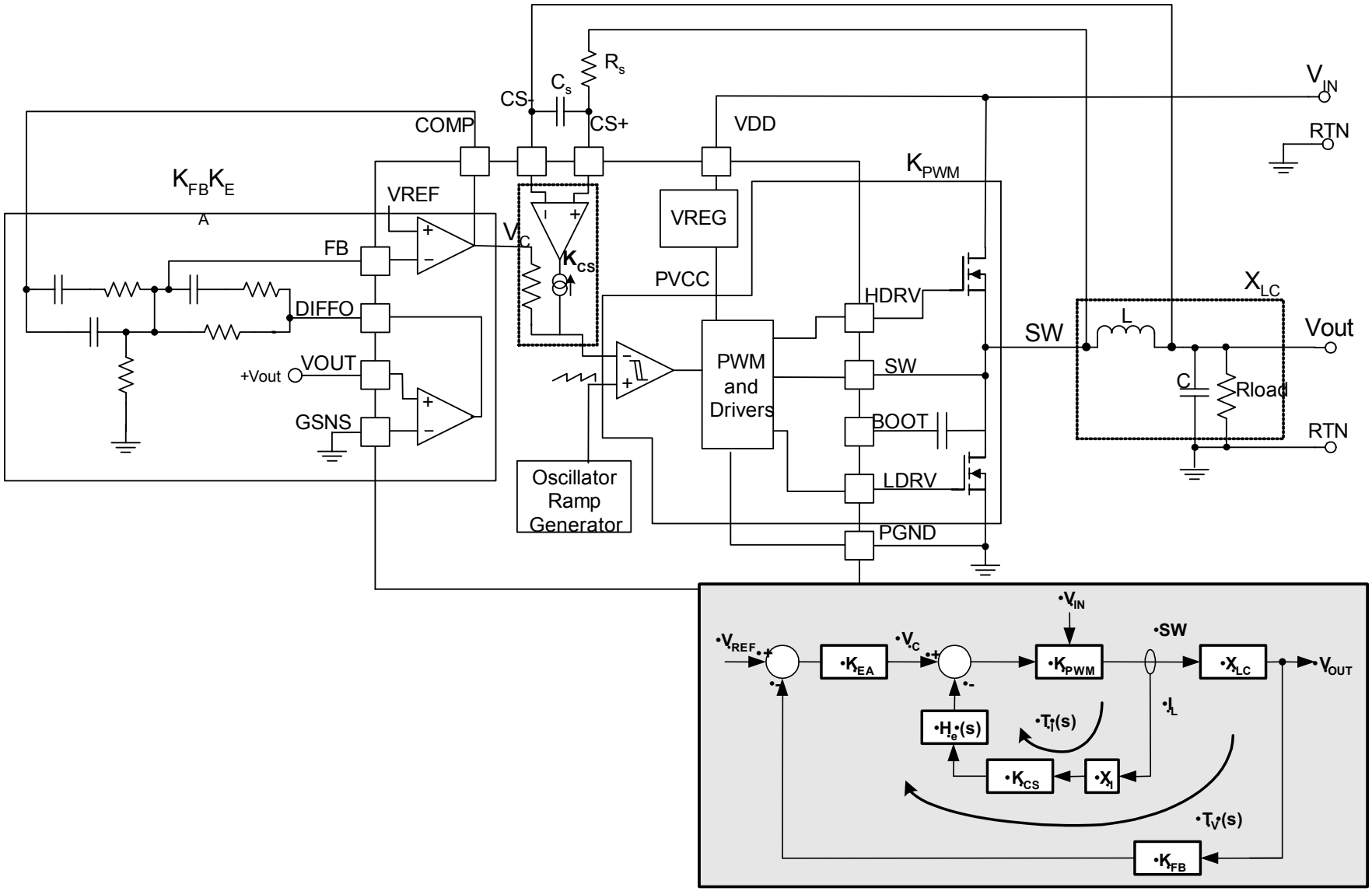


AC CMC Model for Buck Converter

- Peak CMC PWM is the result of a comparison between a control signal, a signal proportional to the inductor current, and a fixed saw tooth (for slope compensation)
- Whether it is:
  - Current feedback and sawtooth vs. control signal
  - Current feedback and control signal vs. sawtooth
  - Control signal and sawtooth vs. current feedback
- From a small signal standpoint, the resulting modulation is the same!

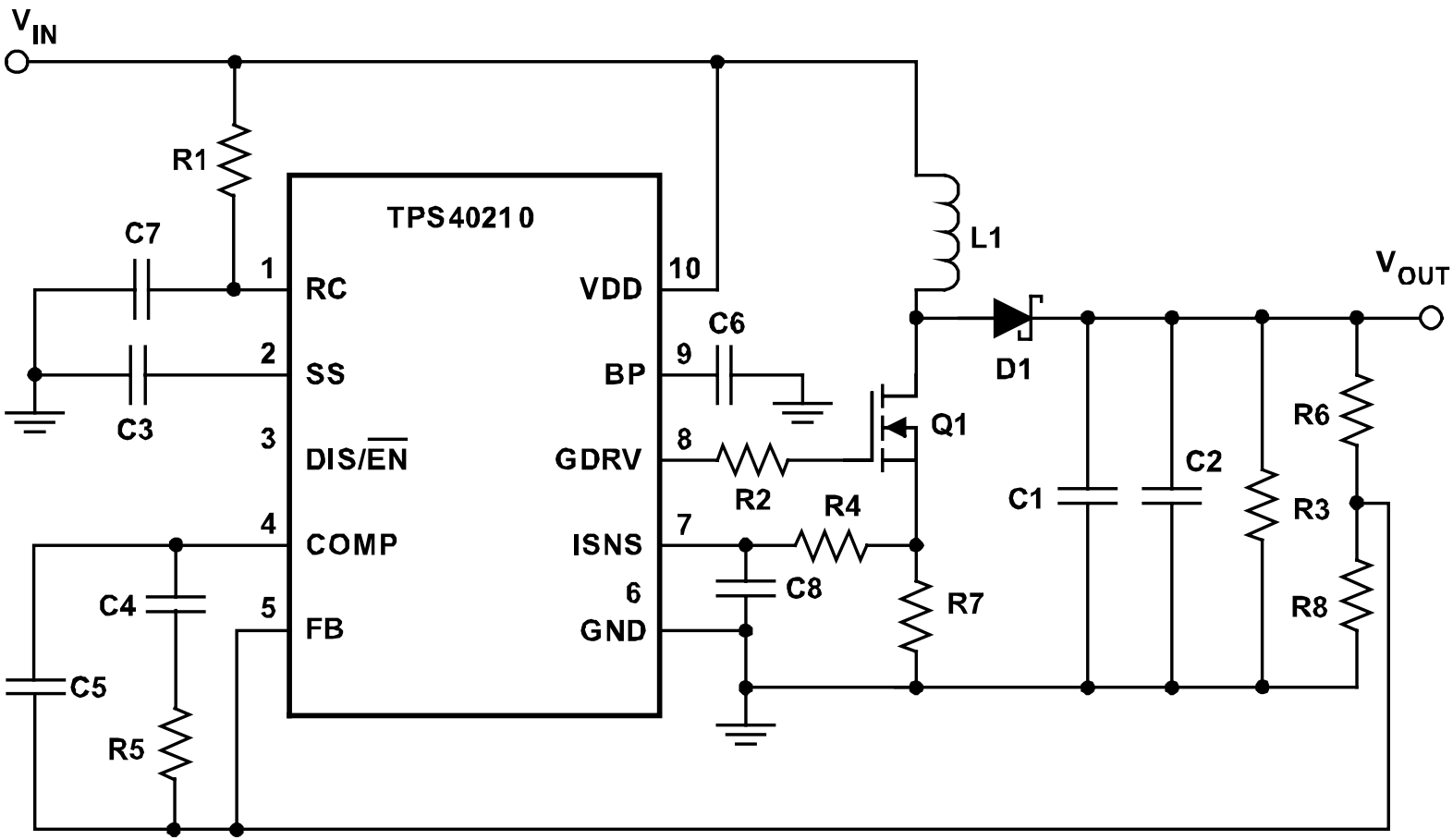


AC CMC Model for Buck Converter



DC/DC Boost Converter

- TPS40210 controller operating ~700 kHz
- 9- to 18-V input (12-V nominal)
- 24-V output with 1-A capability



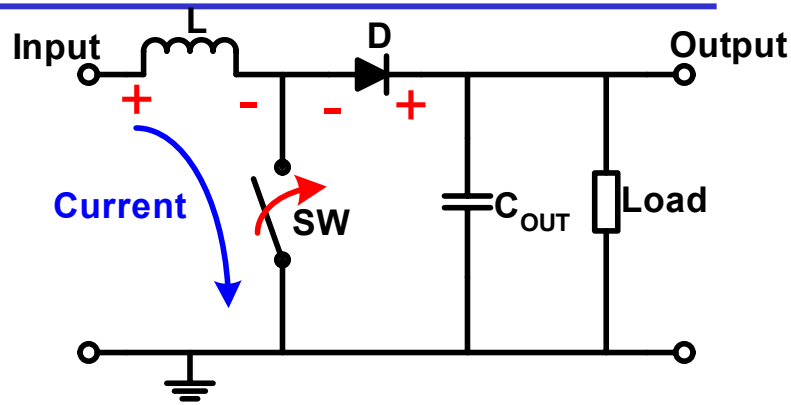
Assumptions in Steady-State Operation

1. V•s balance across the inductor
   - Energy “in” during a period equals energy “out” during the same period
   - Net change of charge in a period is zero

2. Charge balance in the output capacitor
   - Energy “in” during a period equals energy “out” during the same period
   - Net change of charge in a period is zero

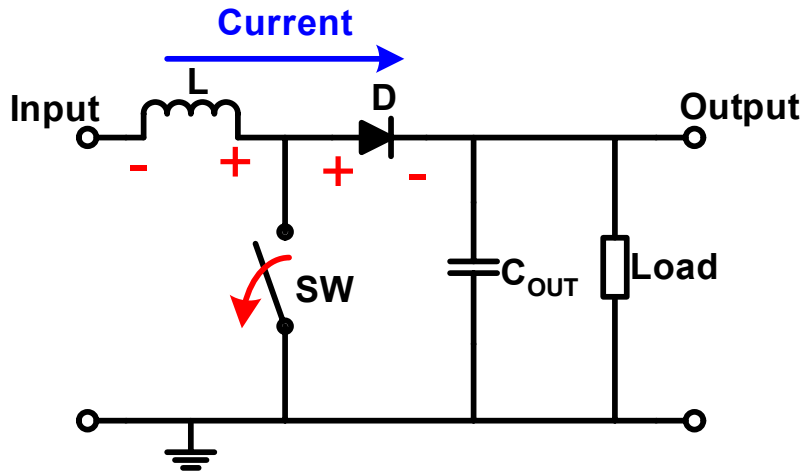
3. Ripple voltage across the capacitor is small compared to the output DC voltage

Basics of Operation



- No switching: $V_{OUT} \sim V_{IN}$
- **SW turns ON:**
  - Voltage across the inductor approaches ~ V_{IN}
    - Energy is stored as function of input voltage, L, t_{ON}
  - D is biased OFF, blocking discharge of the output capacitor
- SW turns OFF:
  - Stored energy is released through D to the output
- Non-pulsating input current – Pulsating output current
  - Level of ripple determined by CCM or DCM operation……

Basics of Operation



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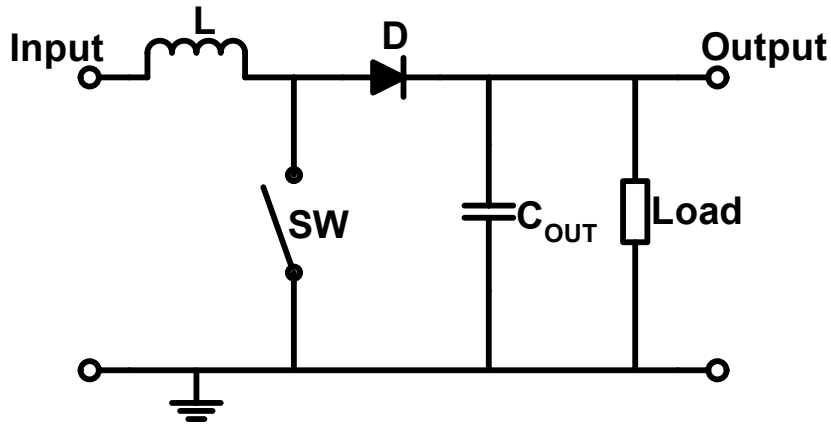
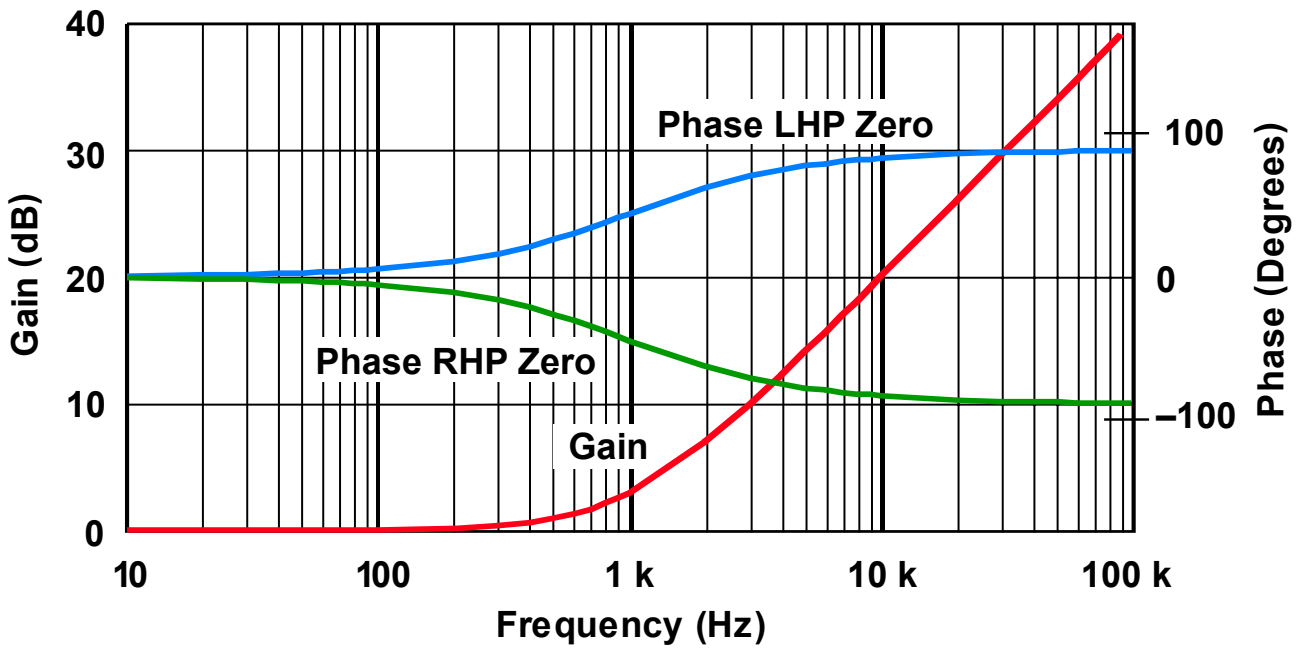
  - Level of ripple determined by CCM or DCM operation……

Right-Half-Plane Zero

- The effect of any control action during the ON time is delayed until the switch is turned OFF
- Output response is initially in the *opposite* direction of the desired correction

  ⇒ RHP Zero





Continuous-Conduction Mode (CCM)

- Switching cycle is composed of two intervals
  1. When the switch is ON, stored energy builds in the inductor
  2. When the switch turns OFF, energy transfers to the output through the rectifier

- Inductor current ON-time slope:

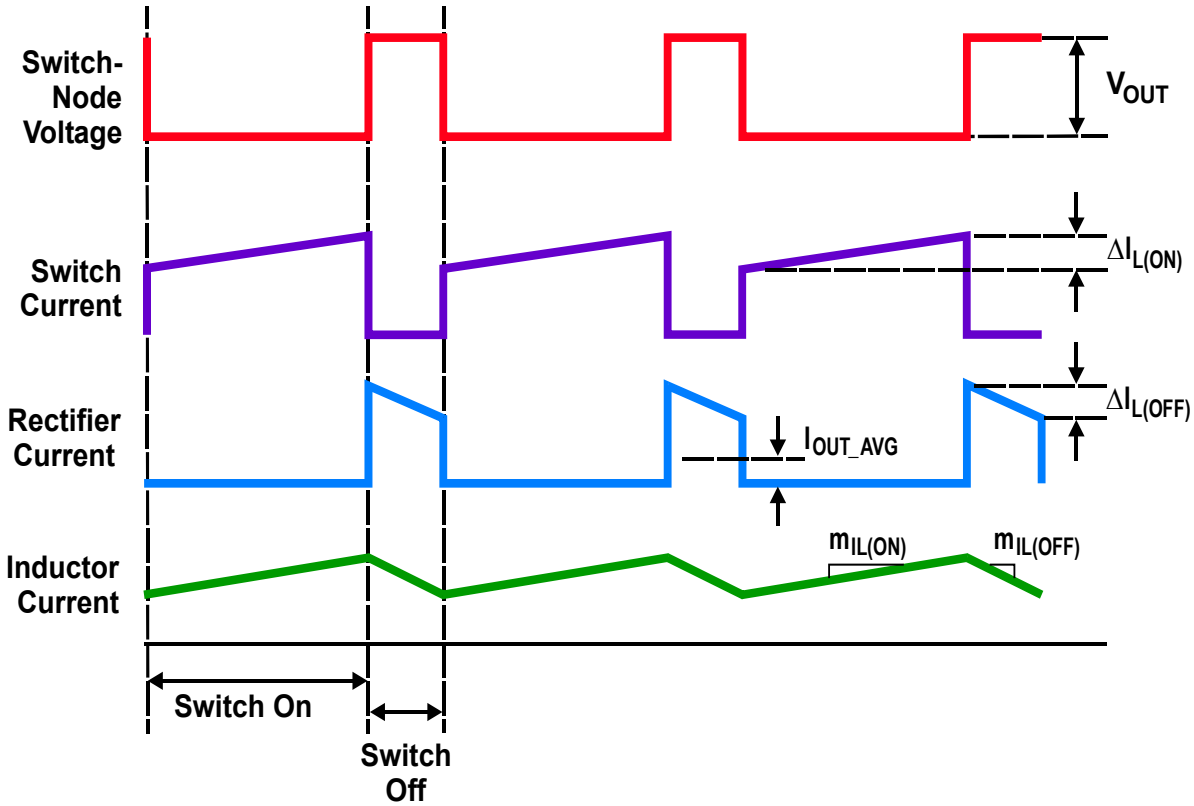
$$m_{IL(ON)} \approx \frac{V_{IN}}{L}$$

- The inductor current OFF-time slope:

$$m_{IL(OFF)} \approx \frac{V_{IN} - V_{OUT}}{L}$$

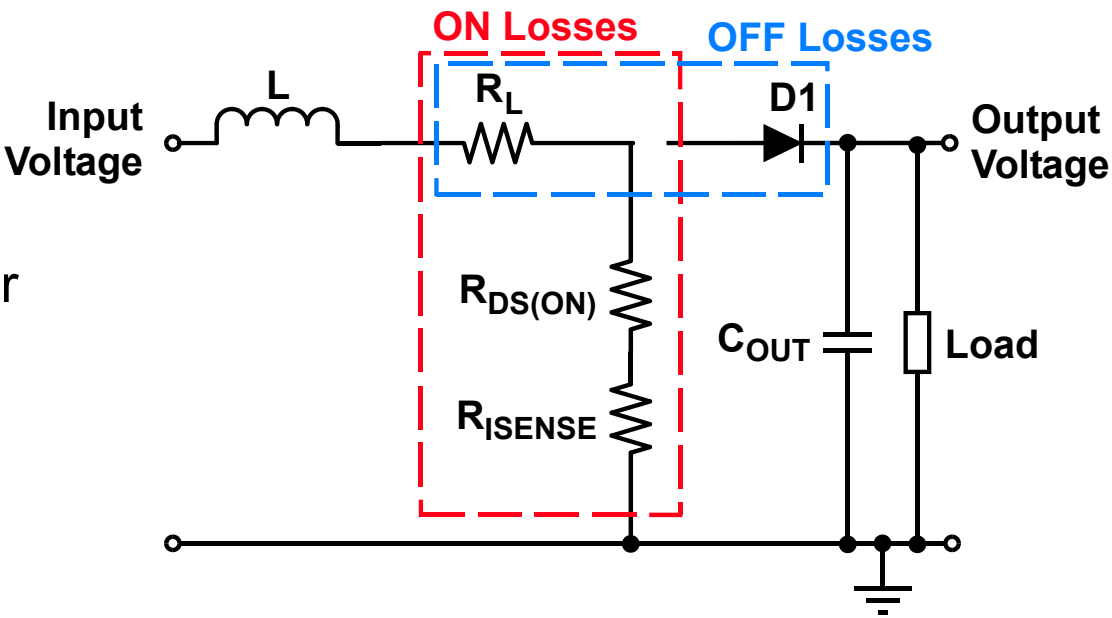
- The switch duty cycle:

$$D_{CCM(ideal)} = 1 - \frac{V_{IN}}{V_{OUT}}$$



Loss Elements in CCM

- "ON" losses
  - Inductor DCR
  - MOSFET $R_{DS(ON)}$
  - Current sense resistor
- "OFF" losses
  - Rectifier voltage drop
  - Inductor DCR



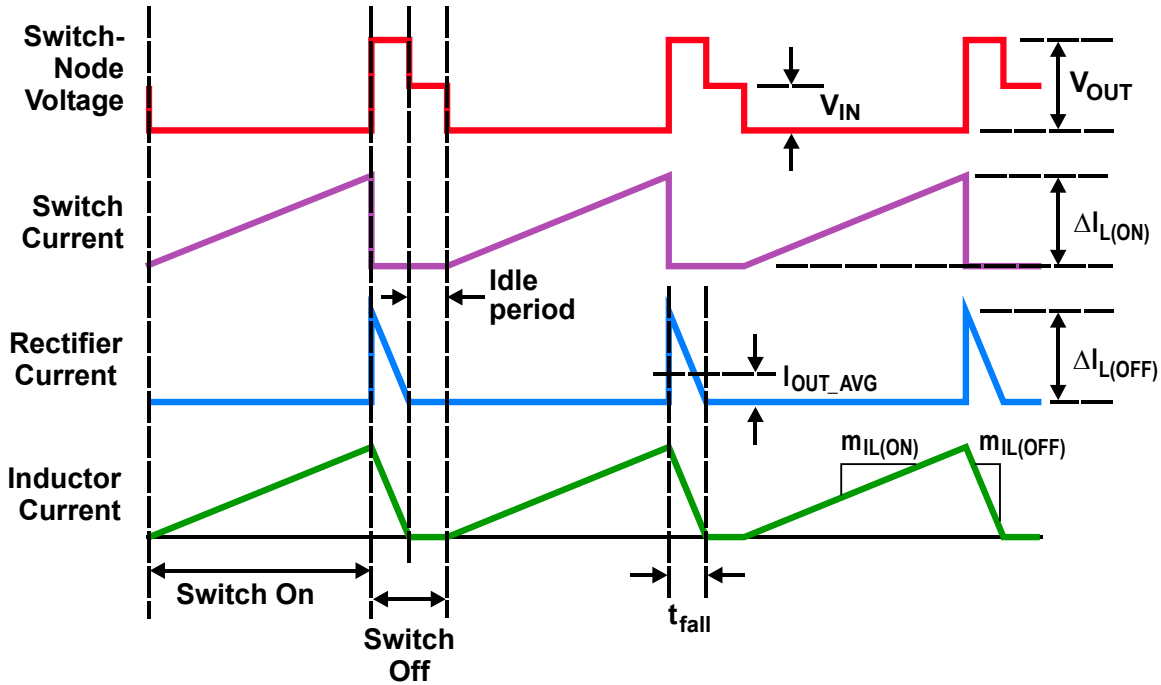
$$D_{CCM} = 1 - \frac{V_{IN} + I_{OUT} \times (R_{DS(ON)} + R_{ISENSE}) + \sqrt{\left[V_{IN} + I_{OUT} \times (R_{DS(ON)} + R_{ISENSE})\right]^2 - 4I_{OUT} \times (R_L + R_{DS(ON)} + R_{ISENSE}) \times (V_{OUT} + V_d)}}{2(V_{OUT} + V_d)}$$

Reduces to $D_{CCM(ideal)} = 1 - \frac{V_{IN}}{V_{OUT}}$ If losses => zero

Discontinuous Conduction Mode (DCM)

- Switching cycle is composed of three intervals
  1. Energy is stored in the inductor during the ON time of the switch
  2. When the switch turns OFF, energy transfers to the output through the rectifier
  3. A third interval during which the energy in the inductor is zero

There is essentially no current flowing in the power stage during the third interval

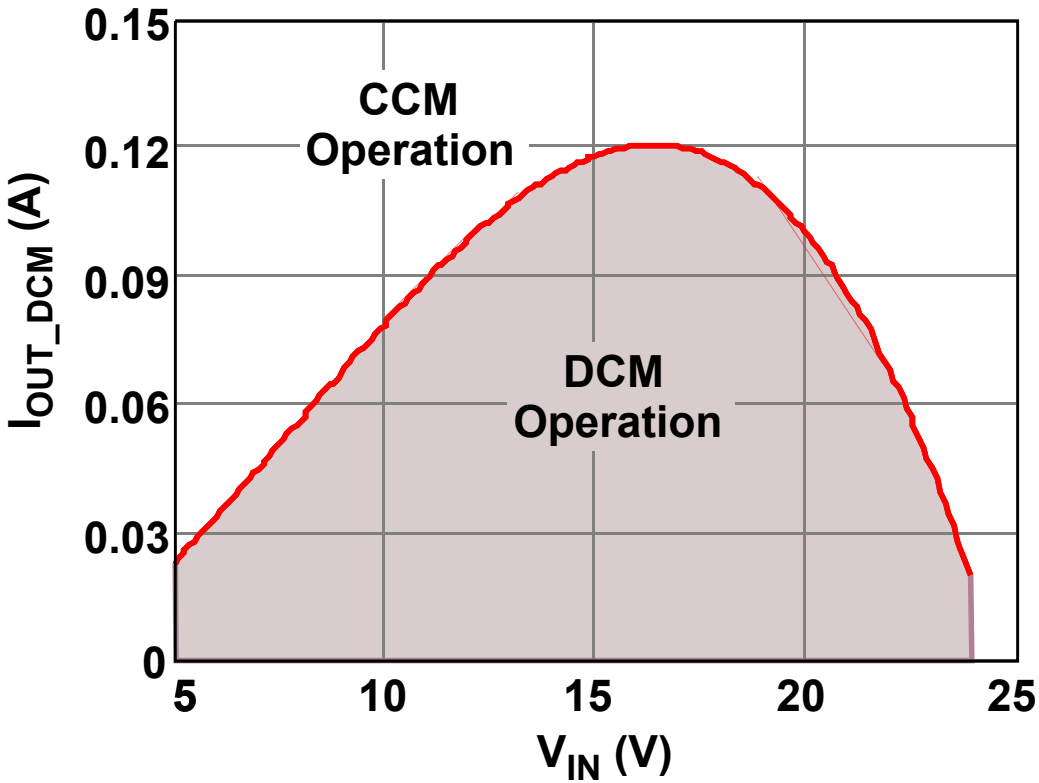


Designing for CCM or DCM

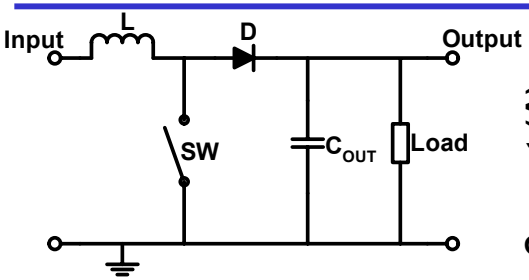
- Given fixed-frequency operation, the only parameter to adjust is the inductance

$$I_{OUT\_DCM} = \frac{V_{IN} \times T_s}{2L} \times D_{CCM} \times (1 - D_{CCM})$$

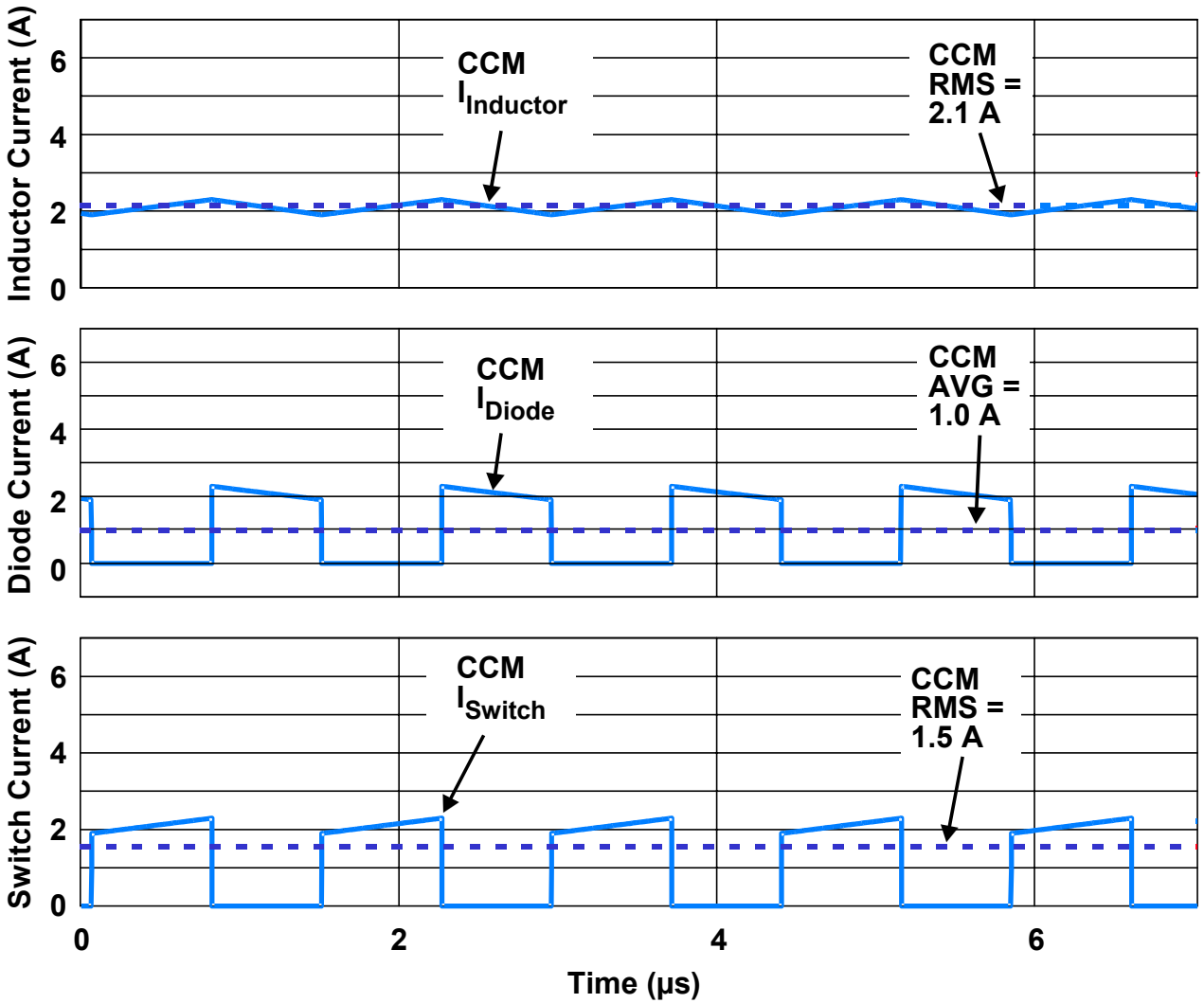
- For a given L, this is the CCM/DCM boundary current



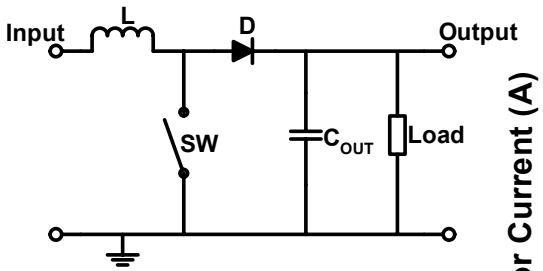
Current in CCM



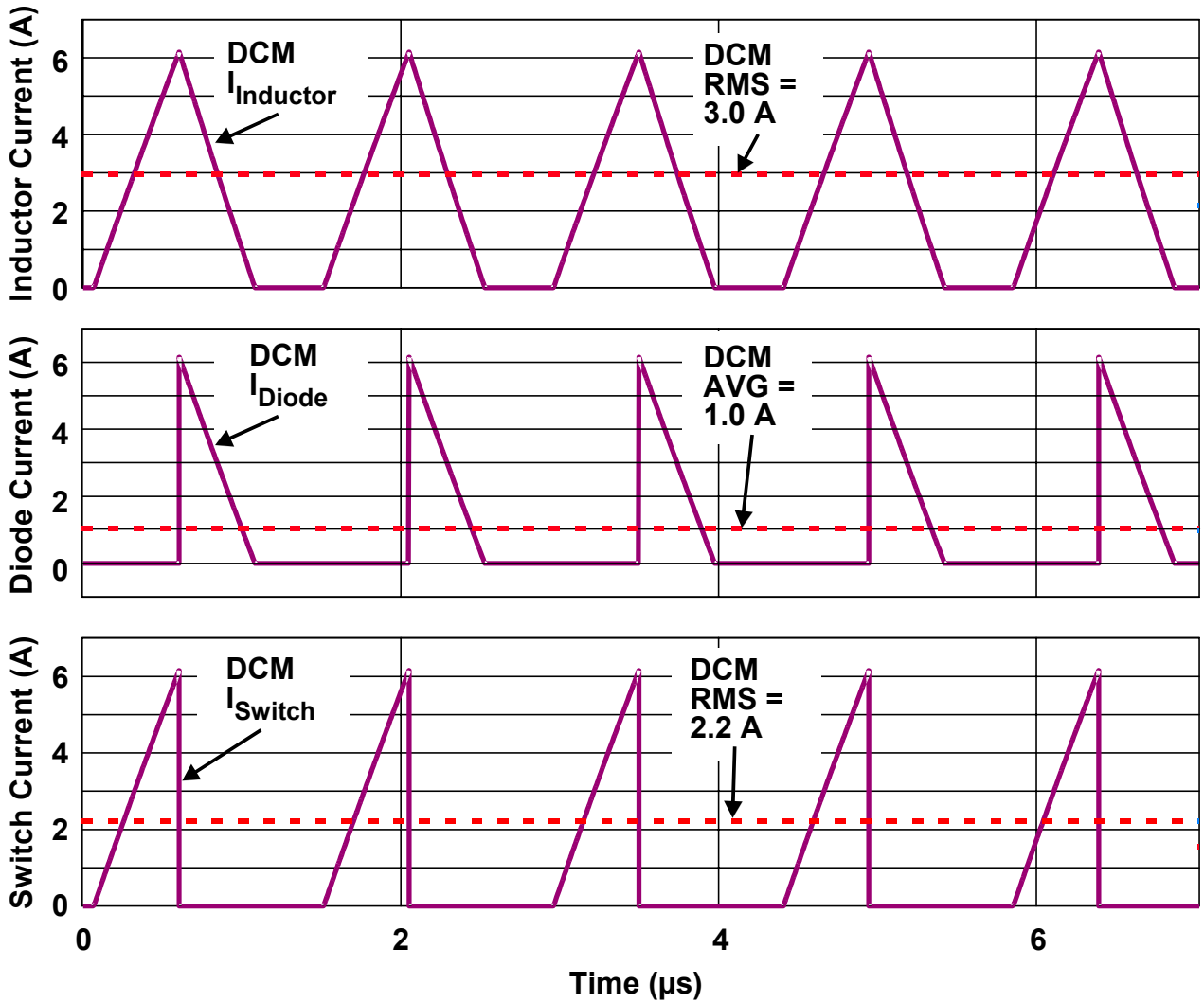
- Continuous current flow in inductor
- Some “pedestal” in diode and switch current
- Diode switching and recovery losses significant in CCM



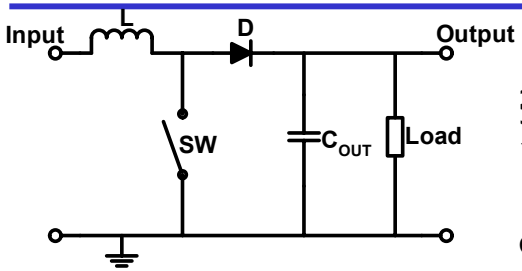
Current in DCM



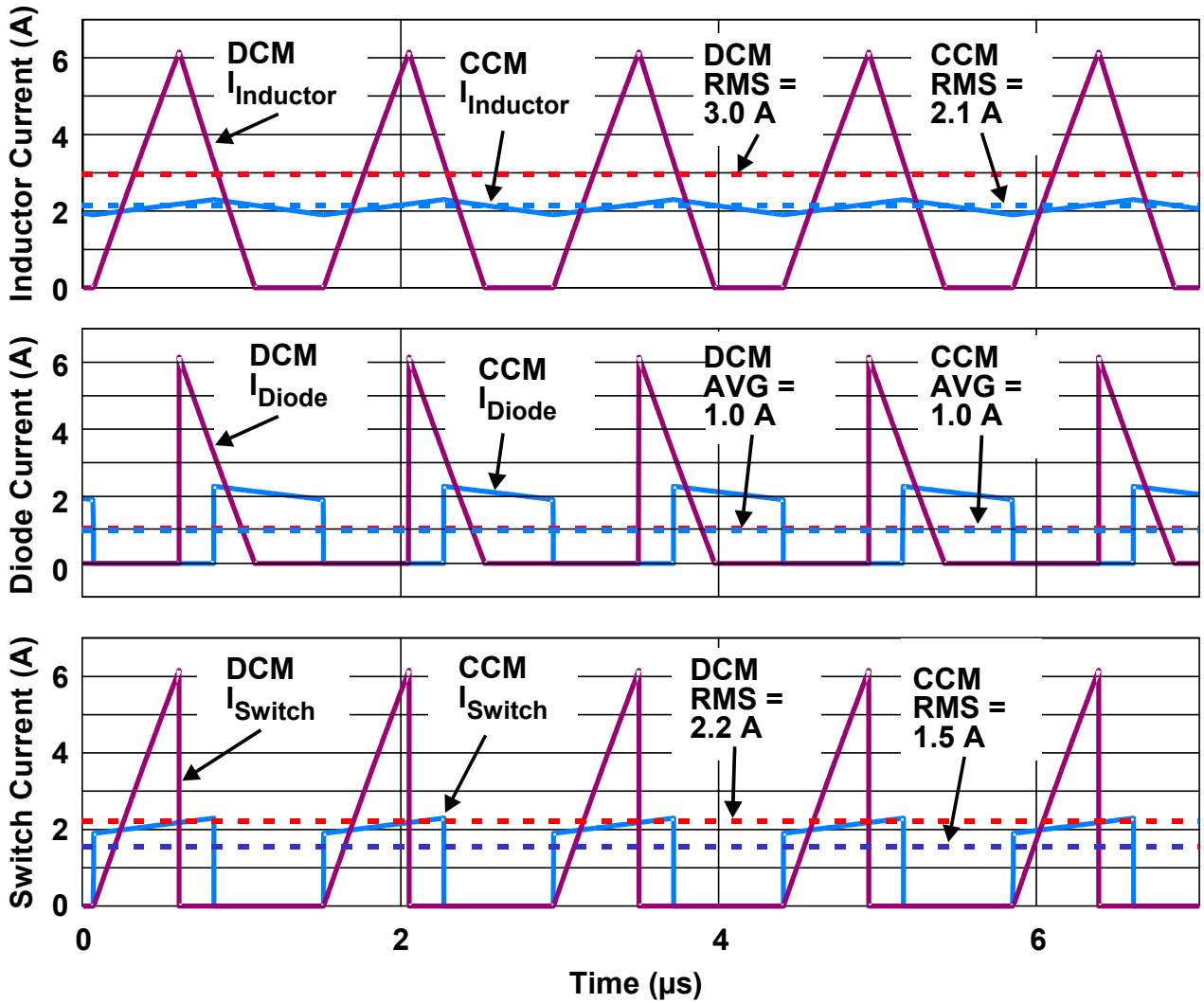
- Large peaks in all currents
- RMS current is higher
- No reverse recovery losses in the rectifier



CCM/DCM - Differences in Current

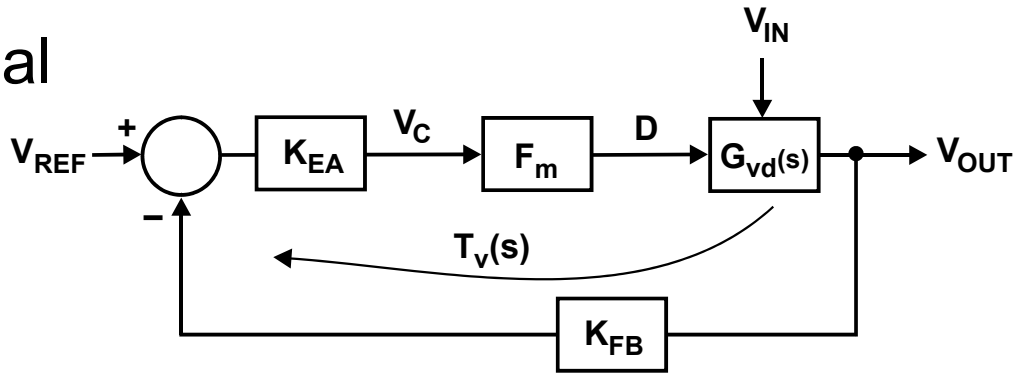


- Peak and RMS currents are larger in DCM
  - Conduction losses will be higher
- Diode-switching and recovery losses will be higher in CCM
- MOSFET turn-OFF losses higher in DCM
- For the diode rectifier, the average current is the same

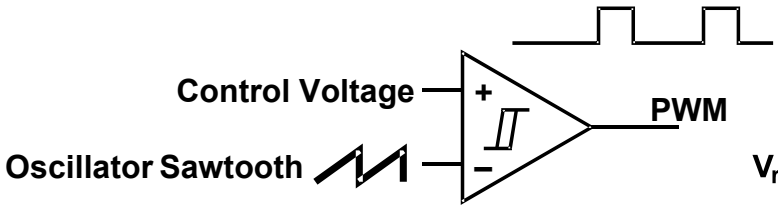


VMC CCM Small-Signal Model

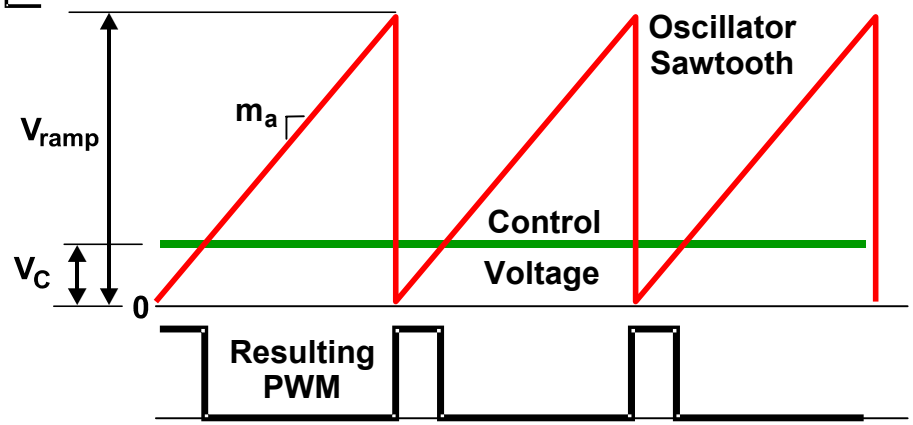
- Simplified small-signal block diagram



- Modulator gain, F_m



$$F_m = \frac{1}{m_a \times T_s}$$



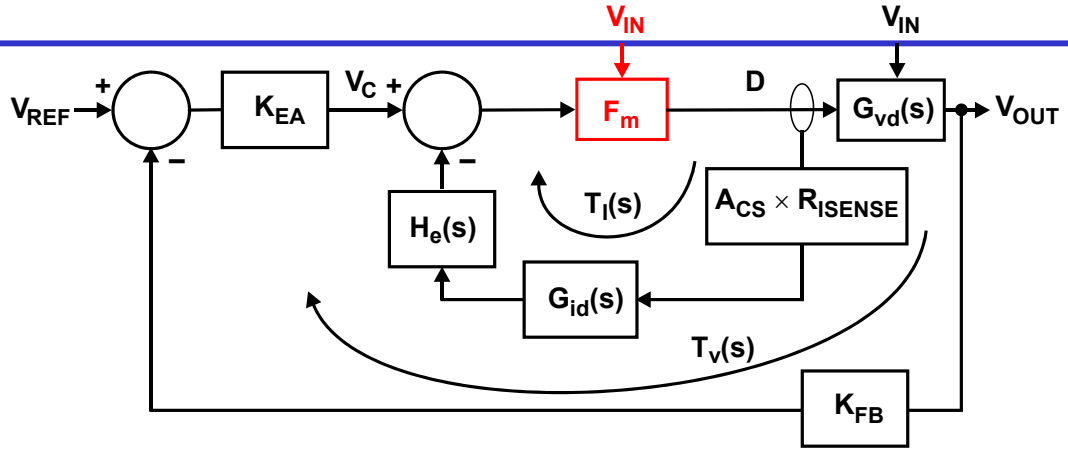
Peak-Current-Mode Control

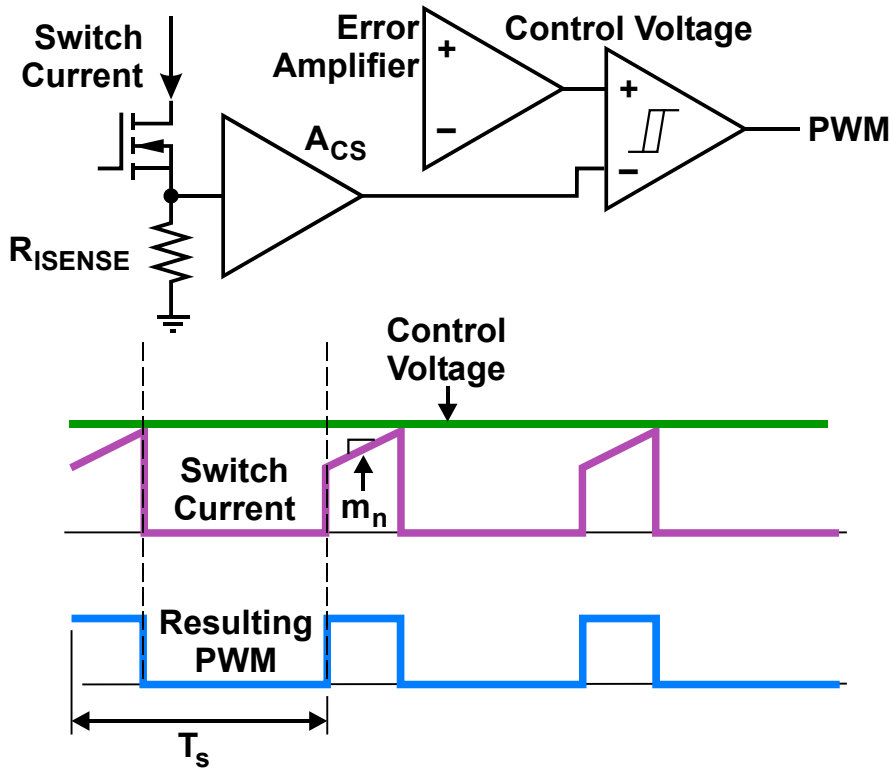
- Modulator gain

$$F_m = \frac{1}{m_n \times T_s}$$

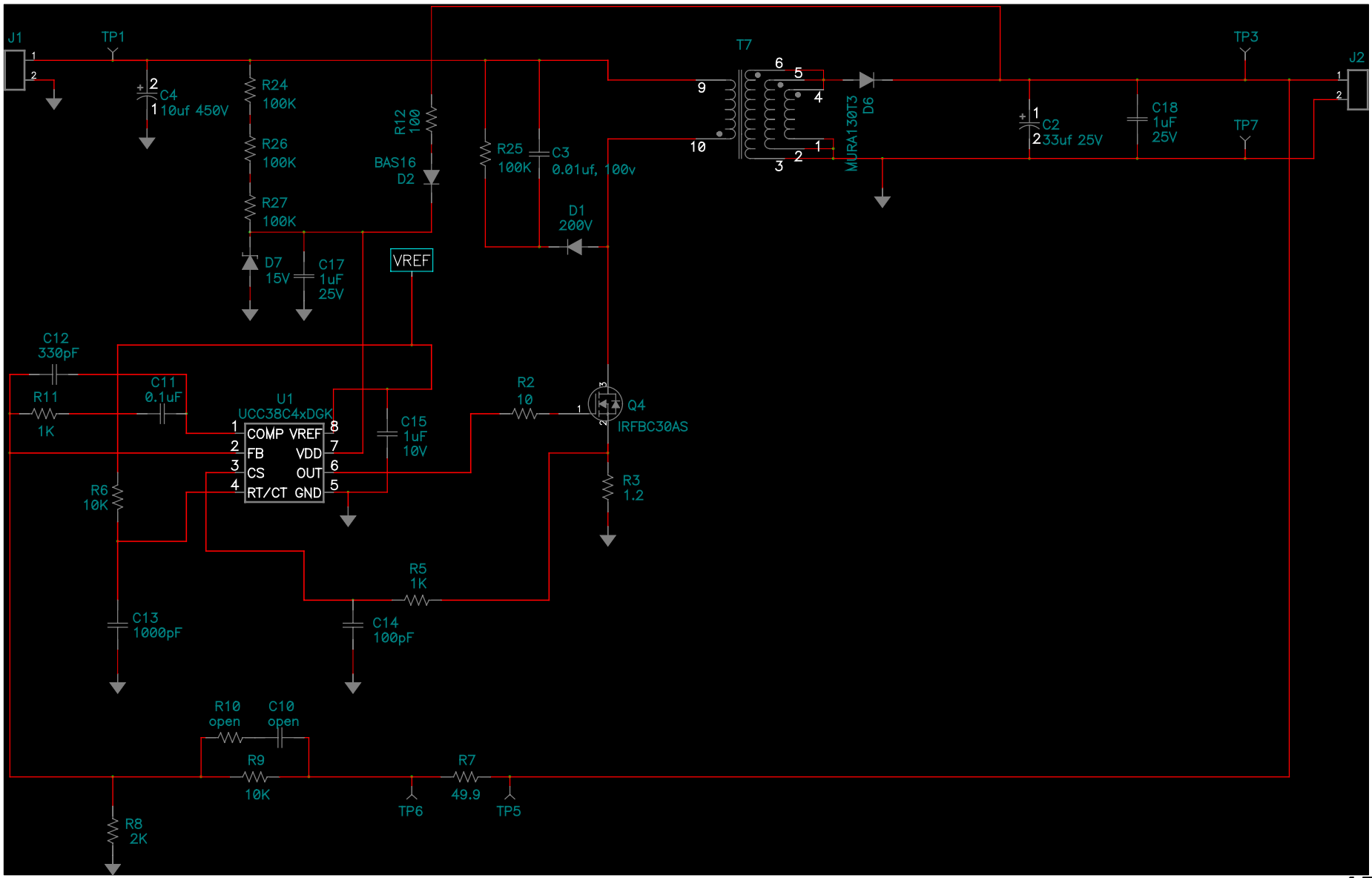
Where

$$m_n = m_{IL(ON)} \times R_{ISENSE} \times A_{CS}$$



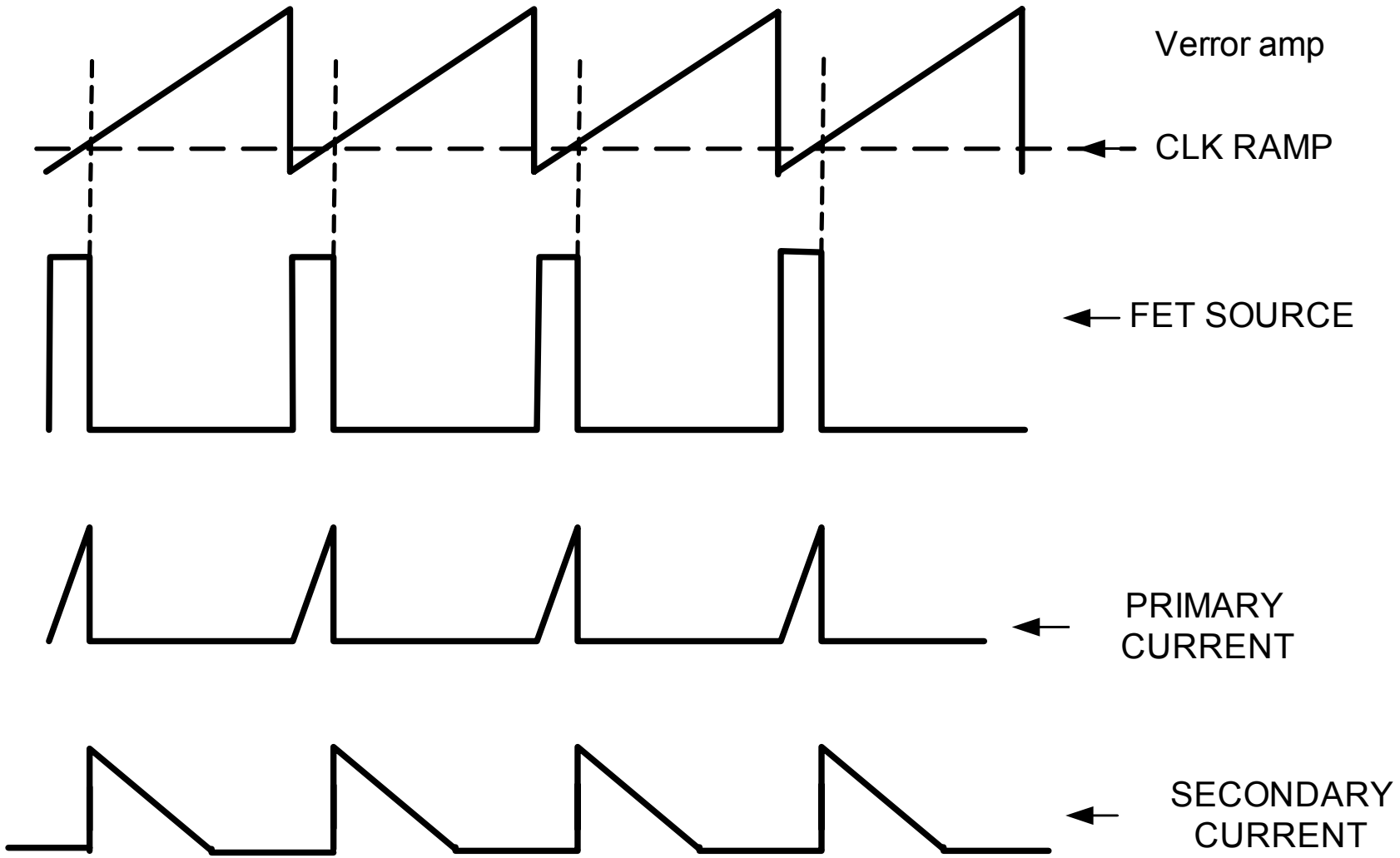


FLYBACK CONVERTER



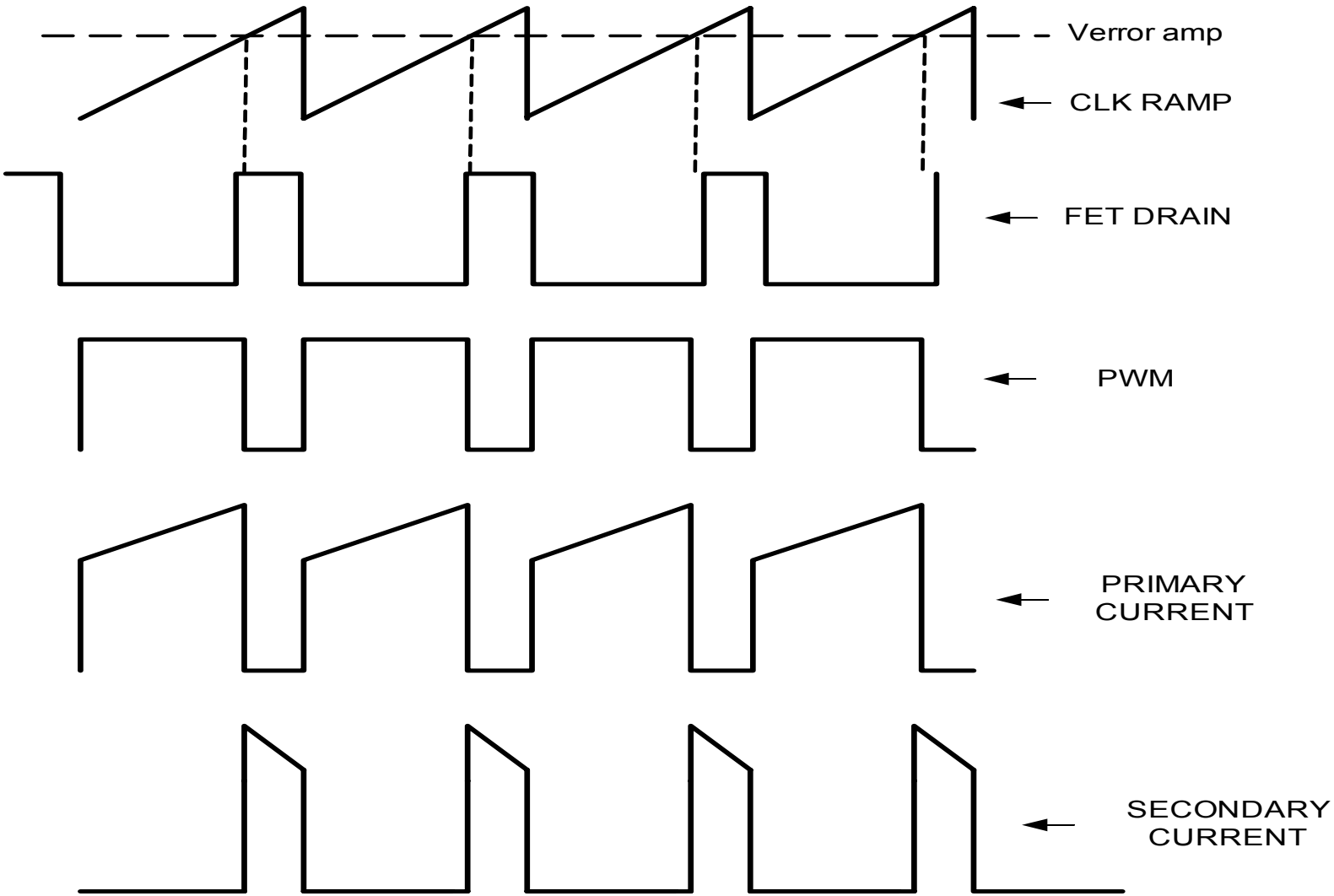
FLYBACK CONVERTER

Discontinuous Waveforms



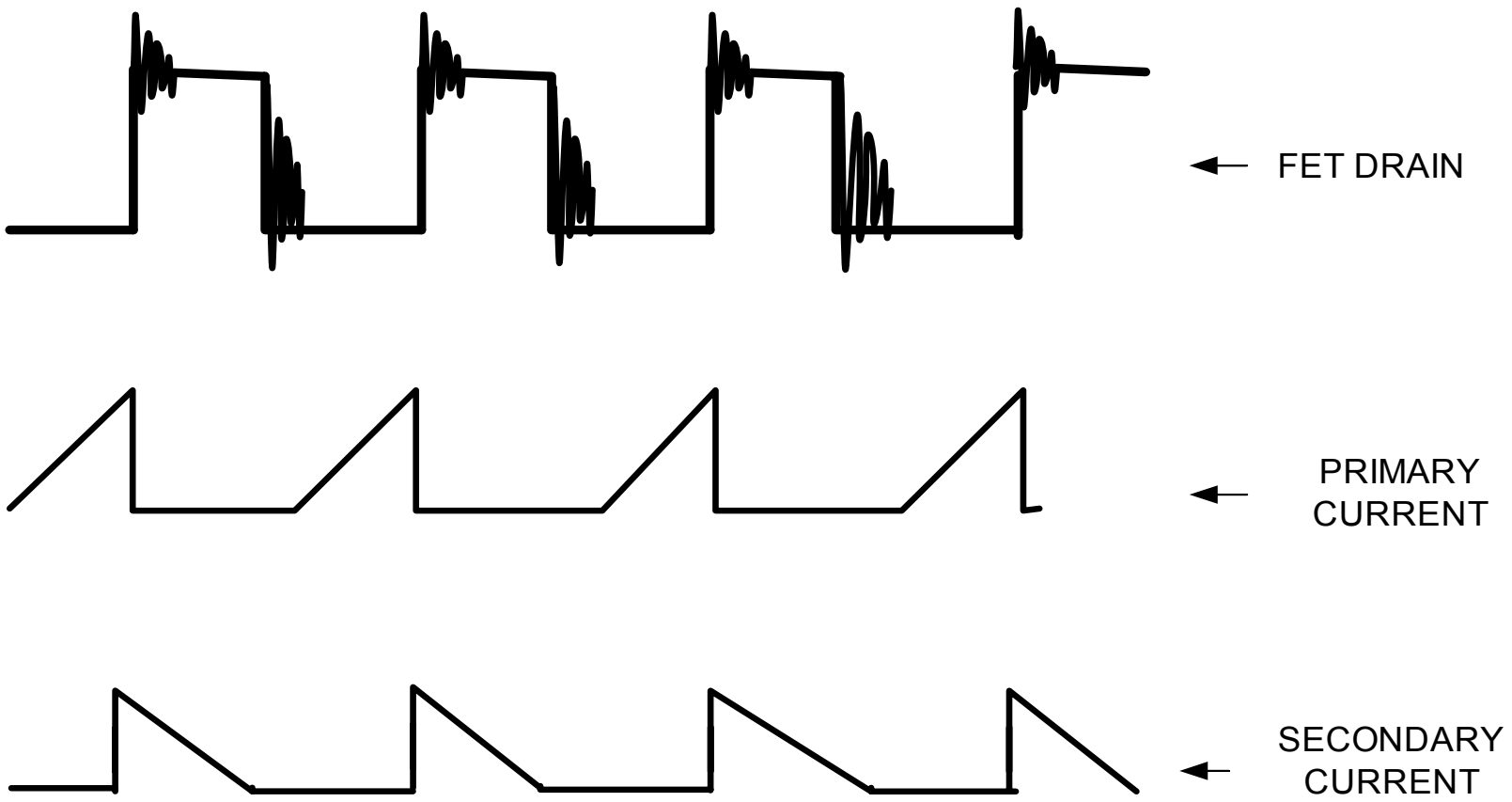
FLYBACK CONVERTER

CONTINUOUS WAVEFORMS



FLYBACK CONVERTER

A ring appears on the drain that is caused by the leakage inductance resonating with the Coss of the switch FET the other ring is caused by the dead time when the transformer is reset and waiting for the next on time.



FLYBACK CONVERTER

Discontinuous

Volt seconds in equals volt seconds out

$$tonmax = \frac{(Vout + 1)(Tr) \cdot .9 \cdot T}{(Vinmin - 1) + (Vout + 1) \cdot Tr}$$

$$V = L \cdot \frac{dI}{dT}$$

$$dI = \frac{Vl \cdot Ton}{L}$$

$$Lp = \frac{(Vinmin \cdot tonmax)^2}{2.5 \cdot T \cdot Pomax}$$

$$Ipri\_p = \frac{Vinmin \cdot tonmax}{Lp}$$

$$Pin = \frac{\frac{1}{2} \cdot Lp \cdot Ip^2}{T}$$

Continuous

Volt seconds in equals volt seconds out

$$tonmax = \frac{(Vout + 1)(Tr) \cdot T}{(Vinmin - 1) + (Vout + 1) \cdot Tr}$$

$$V = L \cdot \frac{dI}{dT}$$

$$dI = \frac{Vl \cdot Ton}{L}$$

$$Lp = \frac{(Vinmin - 1) \cdot Vinmin \cdot tonmax^2}{2.5 \cdot Polow \cdot T}$$

$$Ipri\_ramp = \frac{Vinmin \cdot tonmax}{Lp}$$

$$Icpr = \frac{Pin}{Vinmin \cdot \frac{ton}{Tmax}}$$

$$Ipri\_peak = .5 \cdot Ipri\_ramp + Icpr$$

$$Ipri\_step = Ipri\_peak - Ipri\_ramp$$

SEPIC CONVERTER

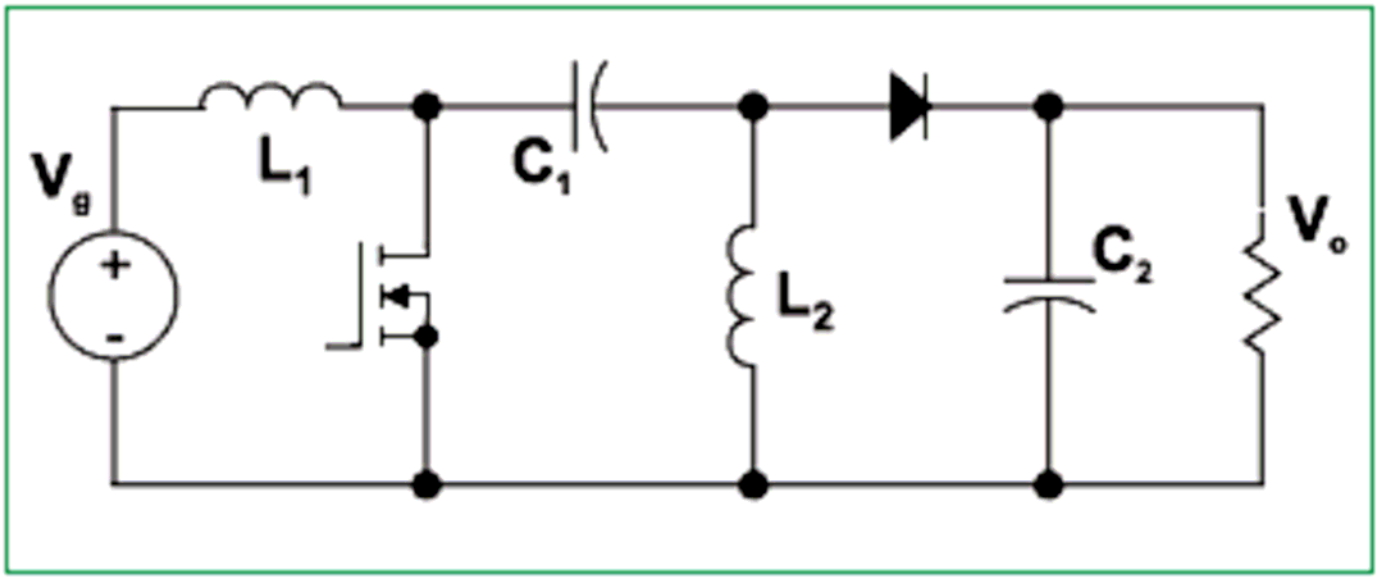


Figure 1. The Sepic converter can both step up and step down the input voltage, while maintaining the same polarity and the same ground reference for the input and output.

SEPIC CONVERTER

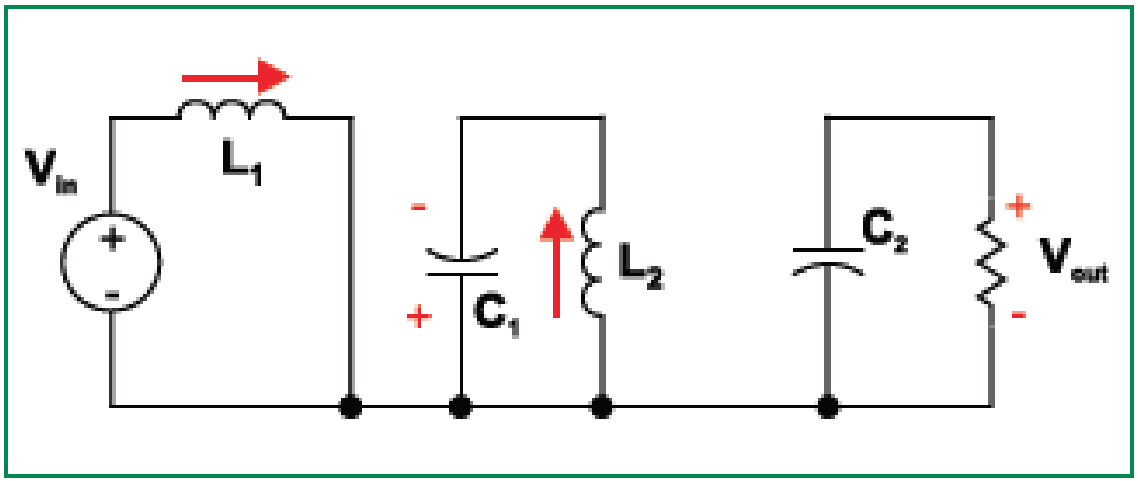


Figure 2. When the switch is turned on, the input inductor is charged from the source, and the second inductor is charged from the first capacitor. No energy is supplied to the load capacitor during this time. Inductor current and capacitor voltage polarities are marked in this figure.

SEPIC CONVERTER

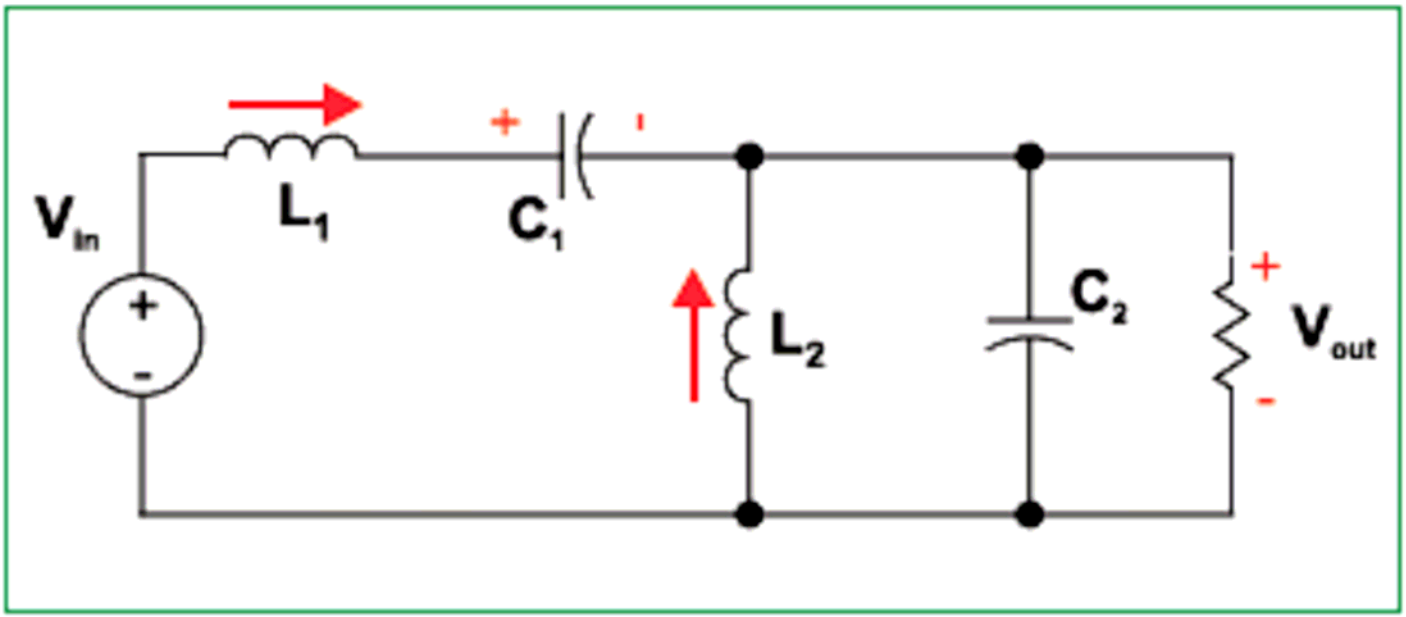


Figure 3. With the switch off, both inductors provide current to the load capacitor.

SEPIC CONVERTER

- Design Equations

$$Duty := \frac{Vout}{Vout + Vin} \qquad I_{L1avg1} := \frac{V_{out} \cdot I_{outmax}}{\eta \cdot V_{inmin}}$$

$$I_{L1pk1} := I_{L1avg1} + \frac{V_{inmin} \cdot d_{max}}{2 \cdot L_{act1} \cdot f_s}$$

- To find an inductor which will keep the converter in the continuous conduction mode this value is used for both inductors

$$L > \frac{Vin \cdot D}{fs \cdot Io \cdot \left(\frac{Vo}{Vin} + 1 \right)}$$

4 SWITCH BUCK BOOST