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Special Focus on Two-Dimensional Materials and Device Applications

Recent progress in devices and circuits based on wafer-scale transition metal dichalcogenides

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Abstract Two-dimensional layered materials (2DLMs) have triggered a broad research thrust over the last decade worldwide. Different from the gapless graphene, transition metal dichalcogenides (TMDs) exhibit versatile bandstructure, with bandgap sizes ranging from semi-metallic to over 2 eV. Therefore, 2D-TMDs can be utilized in various applications from logic to optoelectronic devices. In this review we first introduce the latest developments of the wafer-scale synthesis of continuous TMD films, then we present recent advances in large scale devices and circuits based on TMD films, including logic, memory, optoelectronic and analog devices. We also provide a perspective and a look at the future device applications based on wafer-scale 2D-TMDs.

Keywords two-dimensional layered materials, transition metal dichalcogenides, field effect transistors, wafer-scale

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1 Introduction

Thanks to the research thrust of graphene, a wide variety of two-dimensional layered materials (2DLMs) have also gained much attention during the past few decades [1–4]. As long as the atoms of each layer are combined together by covalent bonds, and van der Waals (vdW) interactions link the layers together, such crystalline materials belong to the huge family of 2DLMs [5–7]. Among various 2DLMs already explored, transition metal dichalcogenides (TMDs) exhibit interesting electronic properties, especially tunable bandstructures which depend on the conditions including material composition, thickness and crystal phases [8–12]. TMDs have a general formula of MX_2, where M and X represents a transition metal (e.g., Mo, W, Pt) and chalcogen (e.g., S, Se, Te), respectively, indicating versatile electronic properties by the combination of various elements (more than 30 TMDs) [13–16]. Moreover, the 2D nature of TMDs allows thickness controlled quantum confinement and vdWs stacking without lattice mismatch, which gives additional degree of freedoms on material engineering for electronic application [1, 17, 18].

Mechanical exfoliation is widely used to prepare high quality mono- or multi-layer TMD sheets in micrometer scale [19–22]. This technique is ideal for fundamental research, including condensed matter physics and nano-chemistry. Most of early prototype devices were fabricated based on this simple and low-cost method [11, 23, 24]. However, low yield and poor reproducibility limit its practical application.

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In order to move TMD based devices from laboratory studies to industrial circuit-level applications, it is more imperative to develop a scalable synthesis method to achieve high-quality, wafer-scale and continuous film. Thus it is essential to develop reliable and controllable synthetic strategy such as chemical vapor deposition (CVD) [25–28], molecular beam epitaxy (MBE) [29–31], metal-organic CVD (MOCVD) [32,33], and atomic layer deposition (ALD) [34,35]. During the past decade, researchers have made great achievements in the preparation of large-scale and high-quality 2D-TMDs samples via the CVD method, which greatly accelerate their practical application. Compared with conventional CVD synthesis methods that use copper film as starting substrate, 2D-TMDs can be directly grown on insulating substrates to avoid the transfer process, which is also an important factor that attracts more research interests [36].

In the past decade, 2D-TMDs drives tremendous research efforts into the field of 2DLM based electronics and optoelectronics. Semiconductive TMD, such as MoS_2, has been widely investigated for demonstration of various devices, especially field-effect transistors (FETs) which is relatively simple to fabricate. Phototransistors have also been intensively investigated due to rich band structures of TMDs [37–40]. Moreover, various TMD based memory devices are demonstrated, including optoelectronic memory [41], dynamic memory cells [42], charge-trapping memory [43], nonvolatile ferroelectric memory [44], static random access memory [45], and semifloating-gate memory [10].

However, most of these devices are based on mechanical exfoliation methods, which prevent them from practical applications. On the other hand, CVD synthesized films exhibit distinctive characteristics from those of exfoliated films, including the existence of more impurities and defects [46, 47], crystalline orientations [48, 49], complex grain boundaries [47, 50, 51], and multilayer islands on the continuous film [27, 52]. Therefore, the electrical transport properties in CVD-synthesized TMD devices usually suffer more charge scatterings, which becomes a major hurdle for achieving high-performance devices. Investigation of wafer-scale homogeneity is also critical for large-scale fabrication of integrated circuits (IC) but only a few related results were reported [48, 53].

Although the exploration of wafer-scale TMD devices is still in its infancy, their fabrication process is more compatible with the traditional CMOS fabrication process, and there is huge room for the improvement of the material quality to significantly promote their future device applications. In this review paper, we focus on the wafer-scale synthesis of continuous TMD films, then present recent advances in electronic and optoelectronic devices based on wafer-scale TMDs, including logic, memory, analog, radio-frequency (RF) and optoelectronic devices. We also provide a perspective and a look at the future development based on wafer-scale 2D-TMDs.

2 Wafer-scale growth of TMDs

In general, 2D-TMDs can be synthesized by two primary strategies: (1) the top-down strategy, where the bulk crystal are physically peeled into mono- or multi-layer sheets by mechanical or liquid phase exfoliation methods; (2) the bottom-up strategy, which is based on chemical reaction to form 2D-TMDs using CVD, ALD, and MBE. Most top-down methods exhibit poor control in terms of thickness, lateral size, and cleanness of the obtained 2D-TMD sheets. To realize practical application, more research efforts have been devoted to the bottom-up synthetic approaches. Among different bottom-up synthetic methods, the CVD method provides a scalable and controllable route for the growth of high quality and wafer-scale TMDs films in a cost-effective manner.

Most CVD growth of TMDs can be categorized into one-step direct deposition and two-step vapor chalcogenization of metal films. For the one-step direct CVD deposition, transition metal-based precursors are evaporated to react with chalcogenide enriched gases to form TMD crystals on arbitrary substrates. Such method can produce high-quality continuous 2D-TMDs in a controllable manner, by playing with various parameters such as growth temperature, furnace pressure, carrier gas flow rate, relative amounts of source precursors, and source-substrate distance. Typical experimental setup of this approach includes a quartz tube containing multiple types of precursors placed in different temperature zones and a substrate mounted in a certain position. Carrier gas like argon or nitrogen is used to deliver the precursors to the

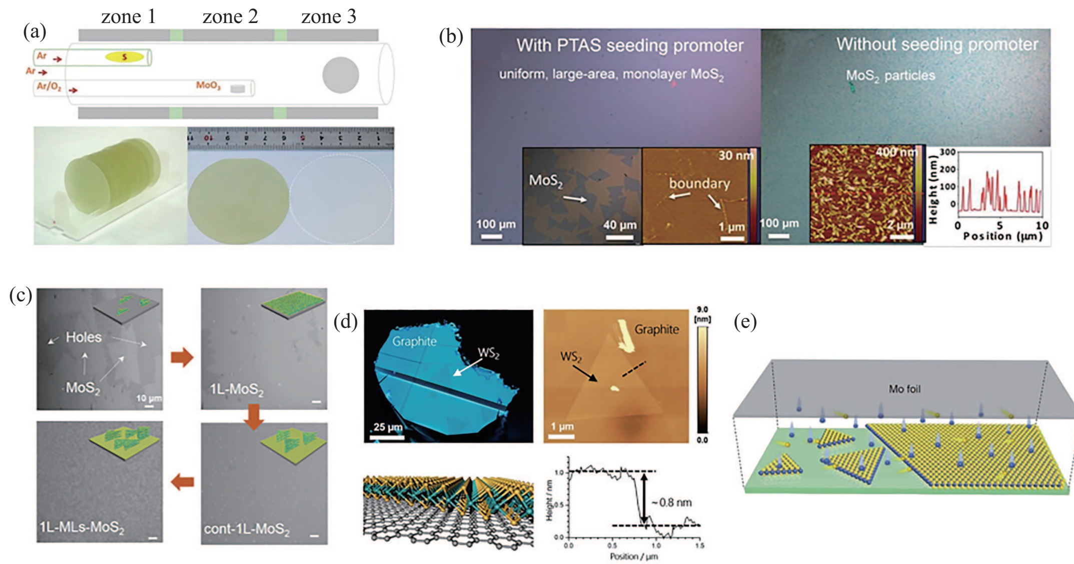

Figure 1 (Color online) (a) Schematic illustration of an experimental setup and photos of 2-inch MoS_2/sapphire and bare sapphire substrate [48] @Copyright 2017 American Chemical Society. (b) The optical image of grown MoS_2 film with PTAS seeding promoter and without seeding promoter. Insets from left to right: optical image of film with PTAS, atomic force microscope (AFM) image of film with PTAS, AFM image of film without PTAS, corresponding height cross-section analysis [54] @Copyright 2014 American Chemical Society. (c) Substrate with not fully covered triangular MoS_2 film, substrate with continuous monolayer MoS_2, continuous MoS_2 film with multilayer starting to grow and continuous MoS_2 film with high-density multilayer islands [55] @Copyright 2016 John Wiley and Sons. (d) Optical image, structure model, AFM image of monolayer WS_2 grown on graphite and height profile along the black line in AFM image [58] @Copyright 2015 American Chemical Society. (e) Schematic diagram of a face-to-face metal-precursor supply route towards synthesizing MoS_2 on glass [36] @Copyright 2018 Springer Nature.

reaction zone. Figure 1(a) depicts an improved CVD system to grow orientated and continuous MoS_2 films [48]. Such system employs independent carrier gas channels for S and MoO_3 precursors for better synthesis control. The epitaxial growth of MoS_2 is highly orientated in wafer-scale with mobility as high as 40 $cm^2V^{-1}s^{-1}$.

The formation of wafer-scale TMD films experiences a series of growth steps, including domain nucleation, domain growth, and domain-domain stitching. To facilitate the nucleation of TMDs, perylene-3,4,9,11-tetracarboxylic tetrapotassium salt (PTAS), 3,4,9,10-perylene tetracarboxylicacid dianhydride (PTCDA), or reduced graphene oxide (r-GO) is pre-coated on the SiO_2/Si substrate [54]. Various other aromatic molecules are also found to be effective as seeding promoters. A large-area, continuous, and high-quality MoS_2 monolayer with domain size around 50 μm is obtained using the PTAS seeding layer. Under the same growth condition without seeding layer, only MoS_2 particles can be produced as shown in Figure 1(b). After the formation of nucleation sites, crystal domains start to grow and coalesce as sulfurization reaction proceeds. The full coverage of the film on substrate is realized by prolonging the growth time as shown in Figure 1(c) [55]. A large fraction of multilayer islands on continuous monolayer is also introduced by pumping the furnace tube to a low pressure. This CVD synthesis strategy realizes the fully continuous MoS_2 film, as well as improving the metal-semiconductor contact during the growth process [27]. The effective mobility of fabricated transistor reaches as high as 70 $cm^2V^{-1}s^{-1}$. For the sulfurization of MoO_3, the reaction typically proceeds in an argon or nitrogen environment. But to realize selenization to obtain $MoSe_2$, it requires stronger reducer such as hydrogen gas, due to the relatively low chemical reactivity of Se [56]. By introducing hydrogen in the reaction environment, highly crystalline WSe_2 monolayer using WO_3 and Se is successfully grown. The hole mobility of as-grown WS_2 is up to 90 $cm^2V^{-1}s^{-1}$, which may shed light on its potential applications.

The choice of growth substrates is also one essential factor that affects the quality of TMDs films [57]. SiO_2/Si and sapphire are some commonly used, some groups have applied graphite [58] and hexagonal boron nitride [29] as the growth substrates for their atomically flat surfaces and thermal stability. Mono-

layer WS_2 film with reduced charged impurities and structural defects is also grown on a cleaved graphite surface as shown in Figure 1(d) [58]. Previous point-to-face metal-source supply method remains difficult for the growth of large-area continuous TMDs films because of the unstable release rates of the metal precursors. To achieve large-scale continuous monolayer TMDs, a novel approach with face-to-face metal source supply has been carried out as shown in Figure 1(e) [36]. A Mo foil is placed above the soda-lime glass at a parallel direction with a gap. The obtained MoS_2 monolayer exhibits an average 200 μm domain size in a continuous form. The achieved mobility of devices fabricated falls in the range of 6.3 to 11.4 $cm^2V^{-1}s^{-1}$, demonstrating the high-quality and uniformity.

For the two-step vapor chalcogenization method, precursors containing transition metal like Mo [59], MoO_3 [60, 61], or $(NH_4)_2MoS_4$ [55] are initially deposited as thin films on the substrate, followed by a chemical reaction in chalcogenide (S, Se or Te) enriched environment at high temperature. This method can produce large-area film with excellent uniformity, mainly because the thin film deposition can be carried out in a controllable manner, by various deposition techniques, including thermal evaporation, E-beam evaporation, ALD, magnetron sputtering, as well as the convenient spin-coating method. The size and number of layers depend on the pre-deposited transition metal based thin films, while the crystalline quality, domain size and defect level depend on the chalcogenization condition. Figure 2(a) [59] depicts the direct sulfurization of Mo metal method. It begins with deposition of Mo thin films with different thickness by E-beam evaporation, and then the Mo film was sulfurized in a furnace in Ar/S atmosphere under a high temperature. This method can reliably produce uniform thin MoS_2 layers with mean mobility 6.5 $cm^2V^{-1}s^{-1}$. An improved electrical contact in which Au contact electrodes is deposited on Mo prior to the sulfurization has been put forward based on this synthetic strategy [62]. Zhang et al. [61] demonstrated tellurization of $MoO_{2.0–2.5}$ and MoO_3 thin films to produce 2H and 1T' $MoTe_2$ according to the phase evolution, and integrated them into functional devices. When it comes to several atomic layers, compared with the physical vapor deposition of Mo or MoO_3, ALD is a more precise film growth technique with atomic resolution. Thus ALD is also utilized for the deposition of the transition metal precursors, as shown in Figure 2(b) [34]. The obtained WS_2 film retains the intrinsic benefits of the ALD process, including controllability of wafer-scale thickness and homogeneity. And the performance of fabricated devices is comparable to that of exfoliated device. The CVD synthesis methods described above require high temperature to realize the chalcogenization step, which is not suitable for plastic substrate. A low temperature compatible method based on solution-processed $(NH_4)_2MoS_4$ is also applied for synthesizing wafer-scale, homogenous MoS_2 thin films. Its two-step decomposition process is put forward as shown in Figure 2(c) [55]. In step 1, $(NH_4)_2MoS_4$ is annealed at 280°C in N_2 atmosphere to decompose into MoS_2. In step 2, MoS_3 is decomposed to form MoS_2 at 450°C under the H_2/N_2 atmosphere. The photo detectors made from as-grown film show a homogeneous photocurrent and good robustness.

At current stage, CVD growth is still limited in research laboratories due to its weak system robustness. To precisely control the growth temperature and the concentration of each reactant, MOCVD technique using gaseous precursors of $W(CO)_6$, $(C_2H_5)_2S$ and H_2 has been reported in 2015 [32], as shown in Figure 2(d) [32]. Such setup shows significant improvement in the controlling of nucleation density and inter-grain stitching, thus producing mobility as high as 30 $cm^2V^{-1}s^{-1}$. TMD films with wafer-scale conformity. FET arrays with a 99% yield and fabrication of vertically stacked multi-level structure are also accomplished, showing great potential of MOCVD technique in the realization of 2D circuits. Other than MOCVD, MBE also shows advantages in controlling and modulating the source supply during the film growth. Scalable monolayer $MoTe_2$ with 100% coverage has been grown on inert SiO_2 substrate. The dynamic-controlled growth can also be extended to synthesizing film on sapphire substrate [61]. Layer-by-layer epitaxial growth of WSe_2 thin film on Al_2O_3 substrates and its ambipolar electronic characteristic has been reported by Nakano et al. [31] Similar epitaxial growth recipe is also applicable for other TMD films as well.

The recent large-scale continuous TMDs synthetic methods are summarized in Table 1. So far, the main challenge to grow high quality continuous 2D-TMD films is the control of grain size. Small grain size is usually correlated with a high density of grain boundaries, which enhance the charge scattering rate and consequently degrade the electrical transport in 2D-TMDs. Moreover, the uniformity of as-

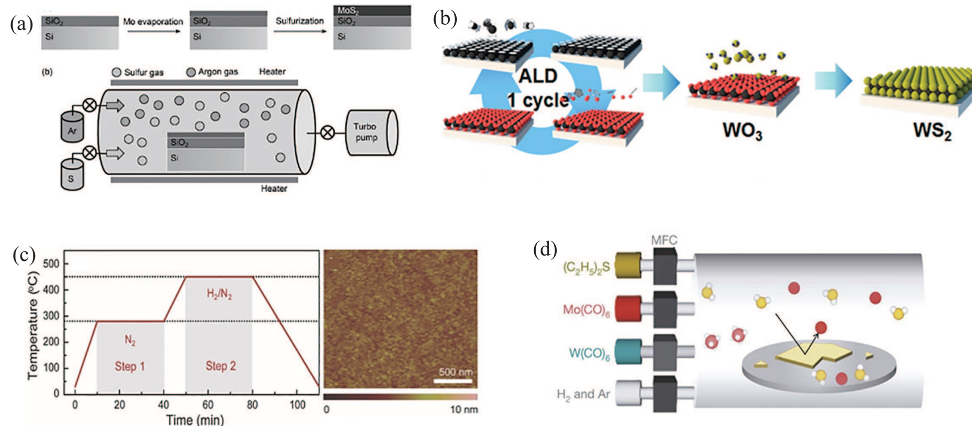

Figure 2 (Color online) (a) A typical setup of wafer-scale MoS_2 growth by sulfurizing of a pre-deposited Mo metal thin film [59] @Copyright 2014 John Wiley and Sons. (b) Schematic illustration of the synthetic procedure for the ALD-based WS_2 film [34] @Copyright 2013 American Chemical Society. (c) Temperature profile of thermal decomposition process for the synthesis of MoS_2 layers and AFM image of the as-grown MoS_2 on SiO_2/Si substrate [55] @Copyright 2016 John Wiley and Sons. (d) Diagram of MOCVD growth setup, precursors were introduced to the growth setup with individual mass flow controllers [32] @Copyright 2015 Springer Nature.

grown films requires further improvement, as it is directly correlated with the device performance and homogeneity. Also, a suitable large-scale transfer method of 2D-TMDs from growth substrates to target ones is also highly desired.

3 Logic devices based on wafer-scale TMDs

3.1 Basic field effect transistors

The downscaling trend of CMOS devices is based on the continuing demand for low power and high performance, but such size scaling is approaching the physical limits for the conventional silicon [63]. A normally considered strategy is to suppress short-channel effect by minimizing the channel thickness to improve the electrostatic control over the channel region. The thickness reduction can be either in vertical or horizontal directions, which correspond to FinFET and ultra-thin silicon-on-insulator (UTSOI) technologies. However, the mobility suffers a severe degradation as the channel thickness scales down due to surface roughness [64–66]. The atomically thin nature of the 2D-TMDs, as well as the preservation of the physical properties under a short-channel condition, can address these challenges [67–69]. Therefore, intensive research efforts have been made to build FET based on TMDs [6, 37, 70–75]. Desai et al. [76] demonstrated a MoS_2 FET with a 1-nm wide gate electrode which is made of a single-walled carbon nanotube (SWCNT), and the device shows a nearly ideal subthreshold swing (SS) of ∼65 mV/decade and large current ON/OFF ratio of $\sim 10^6$.

However, owing to large Schottky barrier and Fermi-pinning effect, electrical contact remains one of the major challenges that limits the performance of TMD-based devices [77]. The contact resistance of a typical TMD FET nearly equals the channel resistance and is generally one order of magnitude higher than that of silicon-based MOSFET. For CVD-grown TMD films such problem is even more severe because of more defects and the existence of grain boundaries. Several research efforts have been demonstrated to reduce the contact resistance, including improvement of metal-TMD contact [78], graphene-TMD contact [79], phase-transition method [80], and adding an extra tunneling layer [81]. Yu et al. [79] first demonstrated a wafer-scale graphene-MoS_2 hybrid structure where graphene serves as interconnect material between MoS_2 and metal electrodes. Kappera et al. [80] presented an intercalation electrochemical method to metallize the contact region for reducing the contact resistance. The butyl lithium is used to functionalize the MoS_2 in the contact region from 2H phase to metallic 1T' phase, and an ultra-low contact resistance of 200 Ω/μm, a high mobility of 56 $cm^2V^{-1}s^{-1}$ can be achieved. Lee

Table 1 Summary of recent large-scale continuous TMDs synthetic methods

Synthetic methods	Materials	Key preparation conditions	Doping type & mobility (cm^2/Vs) & ON/OFF ratio	Domain size (μm) & coverage	Ref.
One-step direct deposition	MoS_2	Independent carrier gas channels	n-type 40 $\sim 10^6$	∼2 100%	[48]
	MoS_2	Aromatic molecules as seeding promotes	n-type – –	∼60 60%	[54]
	MoS_2	Low pressure to introduce multilayer dots	n-type 70 10^8	10–20 100%	[55]
	WSe_2	Introduction of H_2 in reaction furnace	p-type 90 10^5	10–50 –	[58]
	WS_2	Substrate: cleaved graphite surface exceptionally high-temperature at 1100°C	Non-doped – –	15 –	[36]
	MoS_2	Face-to-face metal source supply substrate: soda-lime glass	n-type 6.3–11.4 10^5–10^6	200 43%–100%	[59]
Two-step vapor chalcogenization	MoS_2	Mo metal evaporated by E-beam	n-type 4.1–8.7 –	– 100%	
	WS_2	WoO_3 deposited by ALD	p-type 3.9 –	0.01–0.02 100%	
	MoS_2	$(NH_4)_2MoS_4$ decomposed into MoS_2 at 450°C	n-type 14 5×10^2	– –	[34]
MOCVD	MoS_2	MOCVD precisely control the concentration of precursors	n-type 30 10^6	1 100%	[55]
MBE	$MoTe_2$	Modulating the source supply with mass flow	p-type 32 10^7	– 100%	[32]

et al. [81] improved the electrical contact by depositing a thin T_2O_5 layer between metal contact and MoS_2. The insertion of a 1.5-nm-thick T_2O_5 layer acts as a tunneling layer, which dramatically reduces the Schottky barrier from 96 meV to 29 meV.

Another key issue is the deposition of high quality gate dielectric on the surface of TMD films that provide no dangling bonds [82–84]. The electrical transport in TMD based FETs are significantly influenced by scattering sources including charge impurities, interfacial traps, and defects generated during the ALD process, leading to the degradation of electrical performance. Various technical efforts have been demonstrated to deposit homogeneous high-k dielectrics, such as the insertion of a seeding layer [85], remote plasma treatment [86], and ultraviolet-ozone exposure [87]. Liao et al. [85] reported the deposition of Y_2O_3 on MoS_2 as a buffer layer before the growth of HfO_2 dielectric. A low interface defect density down to $(2.3 \pm 0.8) \times 10^{12}$ cm^{-2}eV^{-1} is achieved and MoS_2 FETs exhibit a large on-state current (526 μA/μm) which is comparable to that of silicon MOSFET. Azcatl et al. [87] utilized ultraviolet-ozone exposure to form O-S bonds on the top surface of MoS_2 without breaking S-Mo bonds. The O-S bonds act as a nucleation layer to allow further uniform depositing of Al_2O_3 dielectric. Other than conventional HfO_2 or Al_2O_3 high-k dielectrics, electrolytes such as ionic liquid [88], ion gel [89, 90] or polymer electrolyte [91], are emerging as alternative dielectrics for gating TMD FETs. The electrolyte gating enables efficient

Fermi-level manipulation by taking advantage of the electric double layer (EDL) effect and the ultrathin nature of TMDs.

Most of the above described methods have only been demonstrated on mechanically exfoliated TMD sheets, and more importantly, these methods either require complicated fabrication procedures or show poor repeatability, which prevent them from practical applications. For CVD-grown large-area TMD films, suitable electrical contact deposition and dielectric layer formation remain unsolved and pivotal challenges, due to the material issues described above [77, 83, 84, 92–95]. Therefore, apart from conventional microelectronic techniques that have been applied to the fabrication of TMD based FETs, it is highly desired to develop compatible device fabrication process aiming for wafer-scale TMD films [69, 70].

3.2 Logic inverter

To advance one step further from a single FET to a logical circuit, inverter is a fundamental building block for the realization of complex digital circuits. The zero bandgap of graphene, which is the pioneering material of 2DLMs, prevents the depletion of charge carriers and limits its applications in digital logic gates [96]. The inability to completely turn off the current through a graphene FET will increases static power dissipation comparing with traditional silicon-based CMOS devices. However, 2D-TMDs shed the light for future application in logic electronics, based on their appropriate bandgap size. In order to build a working logic inverter, the performance of individual TMD-FETs should satisfy basic requirements. For example, current ON/OFF ratio more than 1000 is necessary for the voltage switching, and a moderate mobility is required for high frequency operation. Also, it is necessary to design pull-up and pull-down FETs with matching width to length ratio to obtain suitable switching threshold voltage as well as noise margin for the inverter. So far, because most 2D-TMDs show unipolar behavior, and doping approaches are still immature for wafer-scale TMDs, only n- or p-type FETs can be used for realizing inverter and other logic gates based on one TMD material, other than the complementary MOS technology for conventional silicon transistor.

Amani et al. [97] fabricated an inverter with large-area CVD-grown MoS_2 on flexible polyimide (PI) substrates. Owing to the high n-type doping of the MoS_2, the inverter is integrated in a depletion loaded circuit with a signal gain above 16 at a negative input voltage of -15 V. Xu et al. [27] demonstrated high performance wafer-scale MoS_2 transistors by introducing multilayer MoS_2 islands on the film during CVD synthesis. As shown in Figure 3(a), a pseudo logic inverter is realized using ML-MoS_2 FETs as pull-up and pull-down FETs. The electrical result displays an excellent logic-level conservation and peak voltage gain over 23 at input voltage of -1.1 V. Based on a wafer-scale and high-quality MoS_2 film grown by ALD, Zhang et al. [98] reported the n-type inverter circuits, exhibiting excellent level flip characteristics including switch frequency up to 50 Hz. These studies points out a technical route for potential applications of MoS_2 films in integrated circuit systems.

In addition to MoS_2 based inverter, integrated circuits based on the various 2DLMs or combining 2DLMs with other materials have also been demonstrated. Figure 3(b) shows an optical image of ReS_2 logic gates array (NOT, NAND, and NOR gates). Dathbun et al. [90] demonstrated the realization of NMOS logic devices based on a CVD-grown ReS_2 film with graphene as electrodes. Using the ReS_2 transistors, NMOS inverter is assembled in depletion mode (D-mode) transistor configuration. The inverter operates under a supply voltage of 1 V with a voltage gain over 3.5. Yu et al. [79] demonstrated high performance devices and circuits based on wafer-scale MoS_2-graphene hetero-structure. The integrated inverter is fabricated using two MoS_2-graphene FETs, where MoS_2 and graphene are severed as the transistor channel and contact electrode, respectively. The signal inverter gain is close to 12 within an operating voltage of 3 V. Zhang et al. [61] demonstrated the one-step synthesis of logic gate through the phase-patterned growth of ultrathin $MoTe_2$. After the synthesis process, a PMOS inverter is obtained using two $MoTe_2$ FETs (Figure 3(c)). The inverter is composed of 2H $MoTe_2$ as channels and 1T' $MoTe_2$ as contacts and interconnects. The inverter has an complete rail-to-rail signal inversion and a voltage gain exceeding 35 under an operation voltage of -6 V.

The CMOS inverter, consisting of both NMOS and PMOS, is widely used because it has the advantages

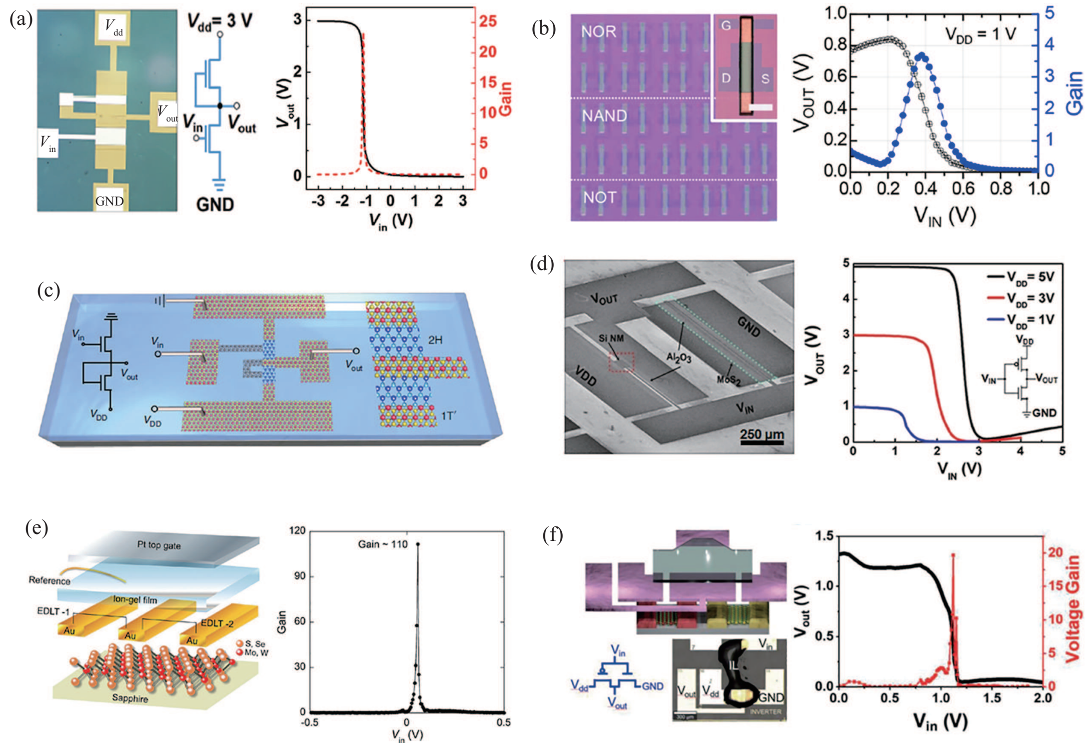

Figure 3 (Color online) (a) Left: the fabricated ML-MoS_2 FET and logic gate array on the wafer. Right: voltage transfer curve and gain of the inverter [27] @Copyright 2018 John Wiley and Sons. (b) Left: optical image of the ReS_2 transistors and logic gates, such as NOR, NAND, and NOT gates. Right: voltage transfer characteristics and signal gain of the NOT gate at $V_{DD} = 1$ V [90] @Copyright 2017 American Chemical Society. (c) Schematic depiction of a chemically synthesized $MoTe_2$ inverter. The left inset is the circuit diagram for the inverter [61] @Copyright 2019 Springer Nature. (d) Left: schematic illustration of a complementary inverter based on Si nanomembrane (NM) and MoS_2 FETs. Right: voltage transfer curves of the inverter at different V_{DD} [100] @Copyright 2016 John Wiley and Sons. (e) Left: illustration of the monolayer MoS_2 and WSe_2 FET built on the sapphire substrate. Right: the voltage gain plotted of input voltage. The maximum gain exceeds 110 with a low input voltage [89] @Copyright 2016 American Chemical Society. (f) Left: schematic illustration along with corresponding optical microscopy image of the CMOS inverter built up on WSe_2 and $MoSe_2$ grown by MGSG. Right: output voltage and gain of the integrated inverter as a function of the input voltage [101] @Copyright 2019 John Wiley and Sons.

of large noise margin and small static power consumption. To form a CMOS inverter based on 2DLMs FETs, transfer method is used to integrate p-type material and n-type channel to make up on the same substrate [99]. As shown in Figure 3(d), Das et al. [100] demonstrated the design and fabrication of CMOS inverters, combing a CVD-grown MoS_2 n-type FET and a Si-NM p-type FET together. The logic inverters, with a maximum DC voltage gain of 16, have been integrated on a plastic substrate to display flexible electrical properties. Pu et al. [89] reported the fabrication of a complementary inverter by transferring p-type WSe_2 and n-type MoS_2 FETs on the sapphire substrate (Figure 3(e)). Such inverter gated by ion gel exhibits the highest voltage gain of 110 so far among other reported 2D materials. Chiu et al. [101] proposed a different method to enable the concurrent growth of two different materials on the same wafer, as displayed in Figure 3(f). Owing to the merits of metal guided selective growth (MGSG) method, it allows the successful synthesis of high quality p- and n-type TMDs for circuit applications. They also demonstrated a bottom-up CMOS inverter composed of p-type WSe_2 and n-type $MoSe_2$ FETs, which exhibited a high voltage gain of 23 independent on the substrate position.

Compared with the strategy of combining two different TMDs together, it's more promising for practical application to obtain n- and p-type channels on the same TMD film, similar to that of conventional CMOS technology. For TMDs with a small band gap that exhibit ambipolar behavior, realization of both n- and p-type FETs has been demonstrated through chemical doping on channel region [28] or choosing different contact metals [12, 102, 103].

Table 2 Summary of TMDs-based inverters

Channel material	Mobility (cm^2/Vs)	Gate dielectric	Substrate	Inverter type	V_{DD} (V)	Inverter gain	Ref.
MoS_2	4.3	35 nm Al_2O_3	Polyimide	NMOS	15	16	[97]
MoS_2	33.73	30 nm HfO_2	Sapphire	NMOS	3	23	[27]
ReS_2	0.9	Ion gel	SiO_2/Si	NMOS	1	3.5	[90]
Graphene & MoS_2	17	20 nm Al_2O_3	SiO_2/Si	NMOS	3	12	[79]
$MoTe_2$	130	12 nm HfO_2	SiO_2/Si	PMOS	−6	35	[61]
MoS_2	3	22 nm Al_2O_3	SiO_2/Si	NMOS	5	50	[9]
MoS_2	7–11	30 nm Al_2O_3	SiO_2/Si	NMOS	5	20	[104]
n-MoS_2 & p-Si-NW	1.3 & 14	50 nm Al_2O_3	SiO_2/Si	CMOS	5	16	[100]
n-MoS_2 & p-WSe_2	30 & 55	Ion gel	Sapphire	CMOS	2	110	[89]
n-WSe_2 & p-$MoSe_2$	11.49 & 10.68	Ionic liquid	Sapphire	CMOS	3	23	[101]
n-MoS_2 & p-MoS_2	10	HfO_2	SiO_2/Si	CMOS	3	22	[12]
n-$PtSe_2$ & p-$PtSe_2$	14 & 15	30 nm HfO_2	Sapphire	CMOS	3	1	[28]

Lan et al. [12] demonstrated both n- and p-type MoS_2 FETs by directly growing MoS_2 film on different types of source/drain silicon electrodes in an identical chip. The p- and n-type MoS_2 FETs are connected as pull-up and pull-down transistors. The obtained CMOS inverter has a high voltage gain over 20. Xu et al. [28] demonstrated a complementary logic inverter based on p- and n-doping $PtSe_2$ film, which was based on the synthesis of wafer-scale continuous few-layer $PtSe_2$ films with controllable p- or n-doping. Using p- and n-type $PtSe_2$ FETs, the complementary inverter is assembled with a voltage gain about 1 under the supply voltage of 3 V. This work opens up a suite of the facile realization of large-scale electronics based on atomic thick $PtSe_2$ film. Recent reports of logic inverter based on TMDs are summarized in Table 2 including voltage gain and the supply voltage.

3.3 Large scale circuits

Besides the continuing improvement of TMD material growth and device processing techniques, another critical challenge is the realization of enhancement-mode (E-mode) FET, which is essential for the realization of multistage cascaded circuits. In previous reports of TMD-based FETs, a significant n-doping effect can be observed and it is usually accompanied with a large negative threshold voltage (V_T) shift in the transfer characteristics. Such effect is mainly due to the interfacial traps, dipoles and charge impurities introduced during the top dielectric ALD growth process [85]. This results in the lack of enhancement-mode TMD transistors with a positive V_T for realization of multistage cascaded logic stages.

To solve this problem, Wang et al. [45] deposited gate metals with different work functions to realize E- and D-mode transistors based on exfoliated MoS_2 flakes. Meanwhile, for large-area CVD-grown TMD films, the gate first technique is adopted [9, 104, 105], in which gate electrodes and dielectric layer are beneath the semiconductor layer as illustrated in Figure 4(a). Compared with conventional gate last technology, gate-first technique obviously improves the performance of MoS_2 FET by minimizing the fixed charges in the gate dielectric. Yu et al. [105] also utilized the gate first technique for the fabrication of highly uniform E-mode MoS_2 FETs and logic circuits. The high-performance E-mode MoS_2 FETs are then used to fabricate combinational logic gates and sequential circuits (AND, OR, NAND, NOR, XNOR, latch and edge-trigger register). The layout and optical photograph of the test chip are shown in Figure 4(b). Owing to the applied gate-first technique, the positive and narrow distribution of V_T is obtained (Figure 4(c)), which is crucial for signal propagation and logic operation in digital circuit. The measurement results of the test chip (Figure 4(d)) show expected logic function of an XNOR gate as well as a latch circuit. This work demonstrated logic gates required in a standard cell library for future synthesis of complex integrated circuits using hardware description languages.

Once the material growth and basic device processing become mature, more research efforts would focus on integrating basic TMD logic gates into functional complicated circuits. As a further step toward the integration of MoS_2 FETs, Wachter et al. [9] presented a 1-bit implementation of a microprocessor,

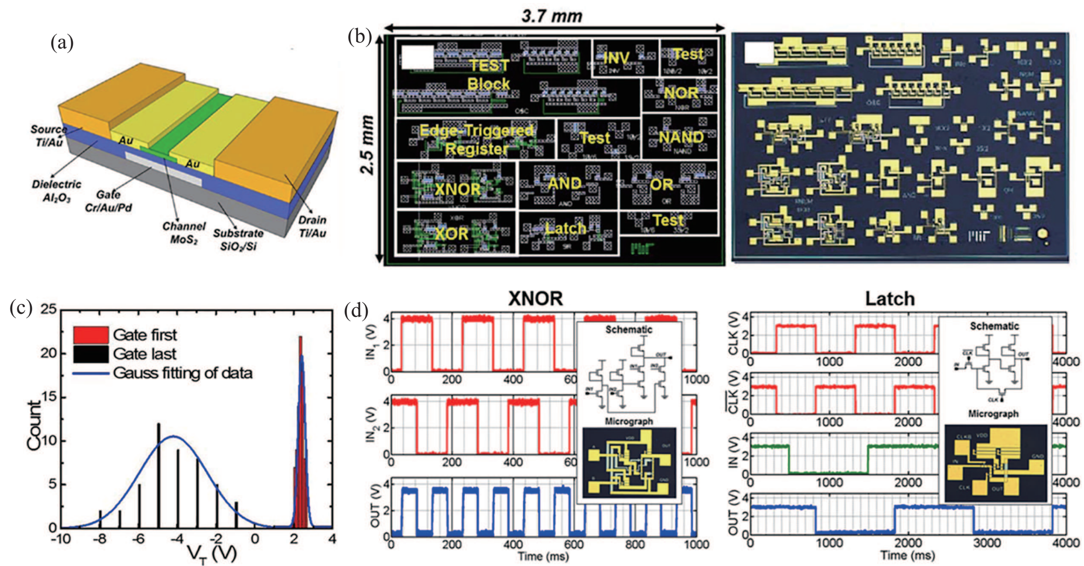

Figure 4 (Color online) (a) Illustration diagram of the MoS_2 FET fabricated by gate-first process. (b) Layout (left) and the optical photograph (right) of fabricated test chip using the design flow. (c) Statistics of V_T of MoS_2 FETs from gate-last and gate-first fabrication technologies. (d) Schematic, micrograph, and waveform results of the fabricated representative XNOR gate (left) and latch circuit (right) [8] @Copyright 2016 American Chemical Society.

which was the most complex circuitry so far made from 2DLM FETs. The circuit is made of NMOS inverters (schematic illustration in Figure 5(a)), where both pull-up and pull-down networks are built by n-type E-mode FETs. The voltage transfer characteristic of the inverter (Figure 5(b)) exhibits excellent performance with a rail-to-rail logic signal conversion. Figure 5(c) displays an optical top-view image of the microprocessor composed of 115 MoS_2 transistors totally. The circuit can load user-defined programs stored in an external memory, to perform simple logical operations and communicate with its periphery (Figure 5(d)). Furthermore, the 1-bit microprocessor is readily scalable to multiple bits operation.

Duan et al. [104] demonstrated high performance electronics on highly uniform solution-processable 2D-TMD nanosheets. The large-area arrays of locally back gated MoS_2 transistors are prepared, which enable the construction of functional logic gates and computational circuits, including an inverter, NAND, NOR, AND and XOR gates, and a logic half-adder (Figure 5(e)). The fabricated logic inverter demonstrates a substantial voltage gain of about 20 (Figure 5(f)). As displayed in Figure 5(g)–(i), logic NAND, NOR, and XOR gates all work at correct functionality. Based on XOR and AND gate, the logic half-adder is designed and fabricated. The data summarized in the measured truth table (Figure 5(j)), show successful operation of a logic half-adder. All these results showing silicon-like performance represent an important step toward future 2D-TMD large-scale electronics.

4 Memory devices based on wafer-scale TMDs

Memory device is essential for digital data storage. Two types of memory devices are commonly used. One is volatile memory, which loses the information stored in it when the external power is turned off. Main volatile memories include dynamic random access memory (DRAM) and static random access memory (SRAM). The other type is non-volatile memory, which preserves its stored data during periods when the power is turned off. State-of-the-art non-volatile memories consist of flash memory, resistive RAM (RRAM), ferroelectric RAM (FRAM), phasec-hange RAM (PCRAM), and magnetoresistive RAM (MRAM). Usually volatile memories have a faster speed than that of non-volatile memories, while non-volatile memories consume less power.

For 2D-TMDs, prototype memory devices have already been demonstrated in the past five years [106–109]. However, so far only RRAM devices are fabricated based on large-scale TMDs. Yang et

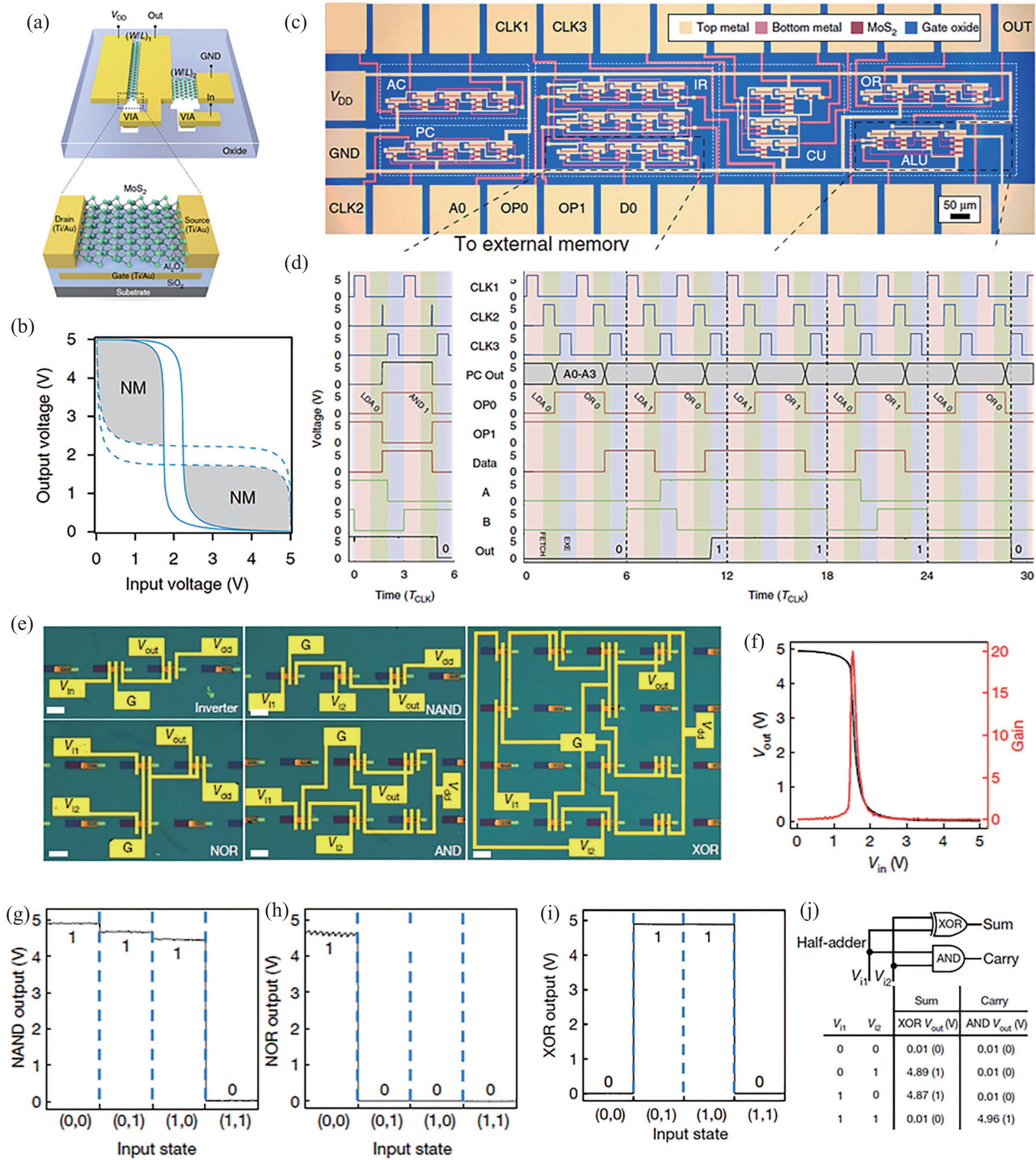

Figure 5 (Color online) (a) Schematic diagram of an inverter (top) and an individual MoS_2 transistor (bottom) in gate-first technology. (b) Output voltage of the MoS_2 logic inverter as a function of the input voltage. (c) Microscope image of the microprocessor containing 115 MoS_2 transistors and measured 0.6 mm^2 in size. (d) Operation timing diagram of the microprocessor [9] @Copyright 2017 Springer Nature. (e) Optical images of an inverter, NAND, NOR, AND and XOR gates on solution-processable MoS_2 nanosheets. (f) The measured voltage transfer curve and signal gain of the integrated MoS_2 inverter. Logic operation of the (g) NAND, (h) NOR, and (i) XOR gates with a power supply of V_{DD} = 5 V. (j) Experimental truth table for the logic half-adder. The logic half-adder is implemented by using an AND gate and an XOR gate [104] @Copyright 2018 Springer Nature.

al. [106] demonstrated a 2T/2R ternary content-addressable memory (TCAM) with CVD growth of continuous, monolayer MoS_2 transistor. The structure of 2T/2R TMD-TCAM cells (Figure 6(a)) utilize each MoS_2 transistor to drive an RRAM element, thus can use far fewer components than SRAM-based TCAM cells. The circuit diagram of the 2T/2R TCAM cell and the searching scheme are shown in Figure 6(c). To store the data bits in the TMD-TCAM cells, the RRAMs are programed by using the 1T/1R scheme. The schematic and the equivalent circuit diagram of the 1T/1R structure are illustrated in Figure 6(b) and (d). Then the RRAM is repeatedly set/reset to HRS/LRS by applying positive/negative voltages on TE (V_{TE}) for 45 cycles by d.c. voltage sweeps (Figure 6(e)), while grounding the source. The 1-L MoS_2 FET can drive enough current to the 1T/1R RRAM, and it is reliably to control the current compliance

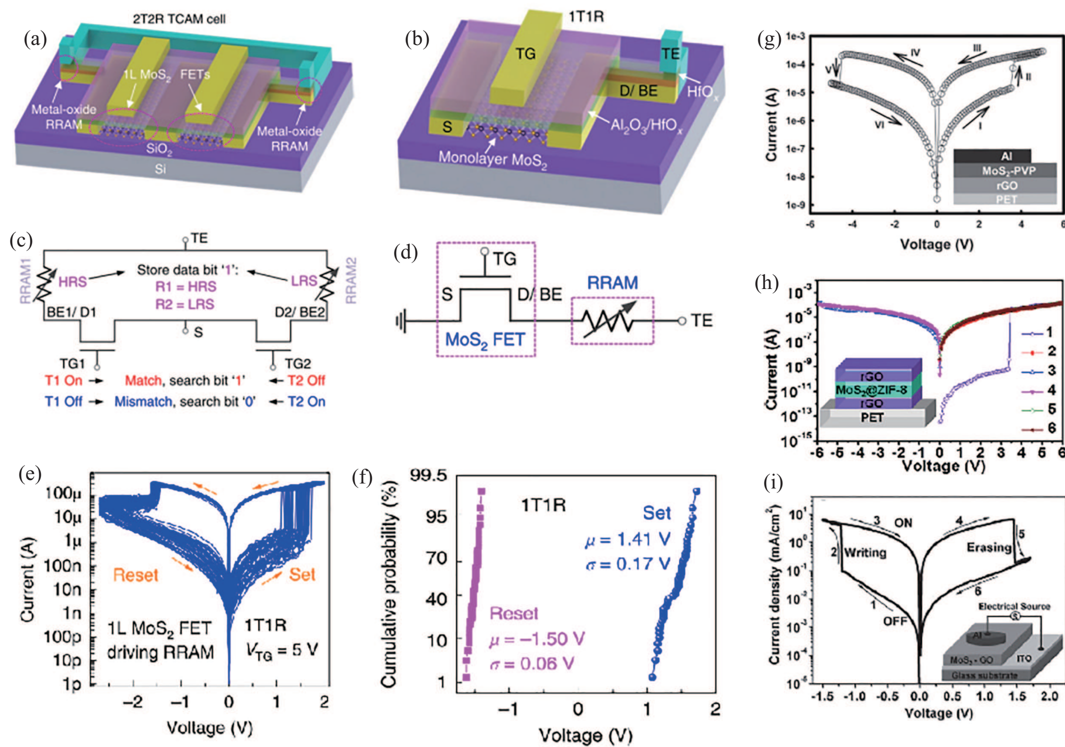

Figure 6 (Color online) (a) The 3D schematic illustration structure of 2T/2R TMD-TCAM cells, using two MoS_2 FET fabricate two RRAM. (b) The 3D schematic of the 1T/1R structure, which is the component of the 2T/2R TCAM cell. (c) Circuit diagram of the 2T/2R TCAM cell based on two RRAM define match or mismatch states with the stored data bit '1' or '0'. (d) Circuit diagram of the 1T/1R structure. (e) Set and reset measurements of the 1T/1R DRAM for 45 cycles. (f) Distribution of the set and reset voltages [106] @Copyright 2019 Springer Nature. (g) I-V characteristics and the schematic illustration of the MoS_2-PVP based flexible memory device [107] @Copyright 2012 John Wiley and Sons. (h) I-V characteristics and the schematic illustration of the MoS_2-ZIF-8 based flexible memory device [108] @Copyright 2014 American Chemical Society. (i) I-V characteristics and the schematic illustration of the MoS_2-GO based memory device [109] @Copyright 2012 John Wiley and Sons.

at the RRAM set process. During the d.c. sweeping, the distributions of set and reset voltages exhibit small variations (Figure 6(f)).

Liu et al. [107] demonstrate a flexible resistive memory device based on MoS_2 functionalized with polyvinylpyrrolidone (PVP). The MoS_2-PVP layer was obtained by direct exfoliation of MoS_2 bulk crystals in PVP solution to form PVP-coated MoS_2 sheets, which was then used as the active layer in a PET/rGO/MoS_2-PVP/Al configuration. Such devices exhibit a typical non-volatile flash memory behavior (Figure 6(g)), with a switching voltage $\sim$3.5 V and ON/OFF current ratio $\sim 10^2$. Another proof-of-concept work was reported by the same research group [108], it demonstrated the switching effect of MoS_2-ZIF-8 on a flexible substrate of poly-ethylene-terephthalate (PET) for memory application. Figure 6(h) shows the current-voltage (I-V) characteristics from the device configuration of PET/rGO/MoS2@ZIF-8/rGO. Then Yin et al. [109] demonstrated a memory device with the structure of ITO/MoS_2-GO/Al, by simply spin-coating the mixture of MoS_2 and GO nanosheets to form the active layer. The resultant memory characteristics display a rewritable switching effect with a switching voltage less than 1.5 V and an ON/OFF ratio of $\sim 10^2$ (Figure 6(i)).

5 Optoelectronics based on wafer-scale TMDs

The working mechanism of optoelectronic devices are based on mutual charge-to-photon conversion process. For the past decade, emerging 2D-TMDs have attracted tremendous research attention for the future application in optoelectronics. One primary reason is that most TMD monolayers are direct band

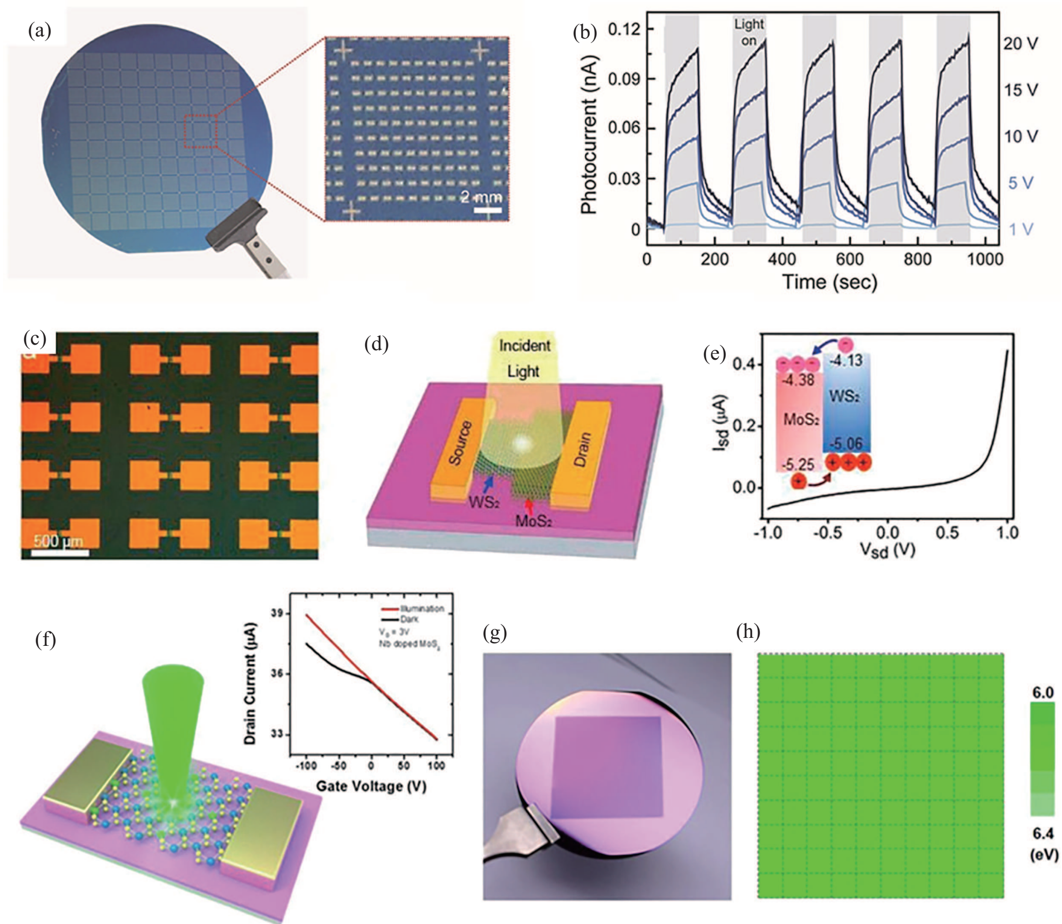

Figure 7 (Color online) (a) Optical image of visible-light photodetector arrays based on homogeneous MoS_2 film on a 4 inch SiO_2/Si wafer. (b) Time-resolved photocurrents of the device measured at P = 12.5 mW×cm^{-2} under different bias voltages [55] @Copyright 2016 John Wiley and Sons. (c) Microscope photograph of MoS_2/WS_2 vertical heterojunction device arrays on the SiO_2/Si substrate. (d) Schematic diagram of the MoS_2/WS_2 vertical heterojunction phototransistor. (e) Current-voltage characteristics of the MoS_2/WS_2 vertical heterojunction phototransistor measured in dark. The inset in (e) shows the band alignment for a WS_2 and MoS_2 vertical heterojunction [115] @Copyright 2016 American Chemical Society. (f) Schematic illustration of the photodetector based on doped MoS_2. The inset in (f): transfer curves of photodetectors based on Nb-doped MoS_2 measured with the exposure of the photodetectors to 282 nW light powers at a 550 nm wavelength laser. (g) Photographic image of a homogeneous large-area film of Nb-doped MoS_2 which was transferred onto a 2 inch SiO_2/Si wafer. (h) Work function distribution across a 5.3 mm × 4.0 mm area divided into 100 regions [116] @Copyright 2019 American Chemical Society.

gap semiconductors, which usually shows higher efficiency of charge-to-photon conversion, compared with that of an indirect band gap. In the recent years, LEDs, photodiodes, photodetectors and solar cells have been intensively investigated based on mechanical exfoliated TMD sheets [110–112]. For wafer-scale TMD films, the optoelectronic study mainly focused on photodetectors [55, 113–116].

Based on a simple two-step thermal decomposition process to prepare wafer-scale and homogeneous MoS_2 sheets from solution-processed $(NH_4)_2MoS_4$ thin films at a low temperature of 450°C [55], the MoS_2 photodetectors were successfully fabricated, as shown in Figure 7(a). The time-resolved photocurrents of these MoS_2 photodetectors are revealed in Figure 7(b), recorded under visible-light at P = 12.5 mW×cm^{-2} for various bias voltages. The response time (the time to reach 90% of the maximum photocurrent after illumination on) and recovery time (the time to reach 10% of the photocurrent after illumination off) of the devices were estimated to be ∼13 and 30 s, respectively. In addition, the homogeneous MoS_2 photodetector arrays also exhibited a homogeneous distribution of photocurrent on the whole wafer. Such MoS_2 photodetectors were also fabricated directly on the polyimide substrate, and the photocurrents decreased only 5.6% after 10^5 cycles of 5 mm radius bending.

In another work, Xue et al. [115] developed a two-step CVD synthesis approach to form a well-defined interface between WS_2 and MoS_2 in the vertical dimension. Figure 7(c) is an optical microscopic image of MoS_2/WS_2 photodetector arrays, spreading out over an area of 25 mm^2. The schematic of a single MoS_2/WS_2 photodetector is illustrated in Figure 7(d). These MoS_2/WS_2 photodetectors show a high photoresponsivity of 2.3 A/W at an excitation wavelength of 450 nm. Figure 7(e) shows a typical I-V curve with an obvious rectifying behavior due to the formation of a junction between the vertically stacked MoS_2/WS_2 heterojunction. The inset of Figure 7(e) schematically shows that electrons can migrate from WS_2 to MoS_2 to form a built-in potential. When a positive bias is applied, the built-in potential is reduced and electrons can easily transport from WS_2 to MoS_2, which results in the on state. When a negative bias is applied, the barrier height at the interface increases to block the electron transport, resulting in a much smaller reverse current. Such property can also be utilized for a self-driven phototransistor without applying source-drain bias. This approach is also transplantable for fabrication TMD heterojunctions with various combinations. Flexible MoS_2/WS_2 heterojunction arrays were also demonstrated, and reasonable photodetection performance was observed.

Kim et al. [116] performed a uniform substitutional doping of monolayer MoS_2 film on 2-inch wafers larger than 13 cm^2. The Nb-doped MoS_2 phototransistors exhibited hole-dominated photocurrent, similar to a p-type semiconductor. The devices also exhibited stable electrical properties in ambient conditions lasting for 30 days. The schematic diagram of the doped MoS_2 under illumination of a focused laser beam is shown in Figure 7(f). Compared with the undoped MoS_2, the optoelectronic performance of doped MoS_2 devices was much improved. The photoresponsivity, detectivity and response rate were measured as 5×10^5 A/W, 5×10^{12} Jones, and 5 ms, respectively. The photo-response time for the rise and decay are 4.9 and 5.7 ms, respectively, slower than 0.63 and 1.63 ms for the undoped MoS_2. In addition, the doping in the Nb-doped MoS_2 film on the wafer (Figure 7(g)) has a good uniformity confirmed by the work function distribution in Figure 7(h). This surprising result showed the feasibility of practical applications based on functionalized 2D-TMDs.

6 Analog and RF applications

In analog applications, FETs have been widely used to mix or amplifier either current or voltage, in which the frequencies of the input signals always fall in the RF range (3 kHz – 300 GHz) or even higher [117]. The research of 2D materials based RF transistors was triggered by graphene. RF transistors perform best in the saturation regime where the conductance of drain can be as low as possible [118]. Unfortunately, the gapless nature of graphene results in no suitable current saturation behavior in graphene-FETs, leading to a major constraint on voltage and power gain [96]. While the mobilities of TMDs are lower than graphene, the appropriate bandgaps in TMDs have resulted in a clear saturation behavior. These properties sponsor TMDs as desirable candidates for next-generation RF applications.

Sanne et al. [119] demonstrated the first CVD-grown MoS_2 device performing at RF (Figure 8(a)). For their monolayer MoS_2 FETs, the short circuit current gain $|h_{21}|$ as a function of frequency shows an extrinsic f_T of 2.8 GHz and an intrinsic f_T of 6.7 GHz (Figure 8(b)). Also, the MoS_2 FETs achieves extrinsic f_max of 3.6 GHz and intrinsic f_max of 5.3 GHz (Figure 8(c)). Furthermore, they demonstrated the implementation of a common-source (CS) amplifier with finished CVD MoS_2 FETs. The frequency of applied signal is 1.4 MHz with 100 mV peak-to-peak voltage, and the output signal is 500 mV, corresponding to a voltage gain $A\mathrm{v} = 14$ dB. Then, an active frequency mixer is also realized, and all the expected harmonics (2RF+LO, 2LO-RF, . . .) are clearly found.

But so far, all the studies had done were on rigid substrate, until one year later in 2016, Chang et al. [120] had finished RF performance for CVD-grown MoS_2 FET on flexible substrate (the inset in Figure 8(d)). For the device on the flexible substrate, intrinsic f_T is 5.6 GHz and intrinsic f_max is 3.3 GHz. Again, CS amplifier with 15 dB gain (Figure 8(e)) and RF mixer (Figure 8(f)) are achieved. However, the applied frequencies remain 1.4 MHz. As shown in Figure 8(g), a MoS_2 FET-based wireless AM receiver is designed in this work, and performances clear signals at 500 kHz. The MoS_2 FET multiplies the carrier

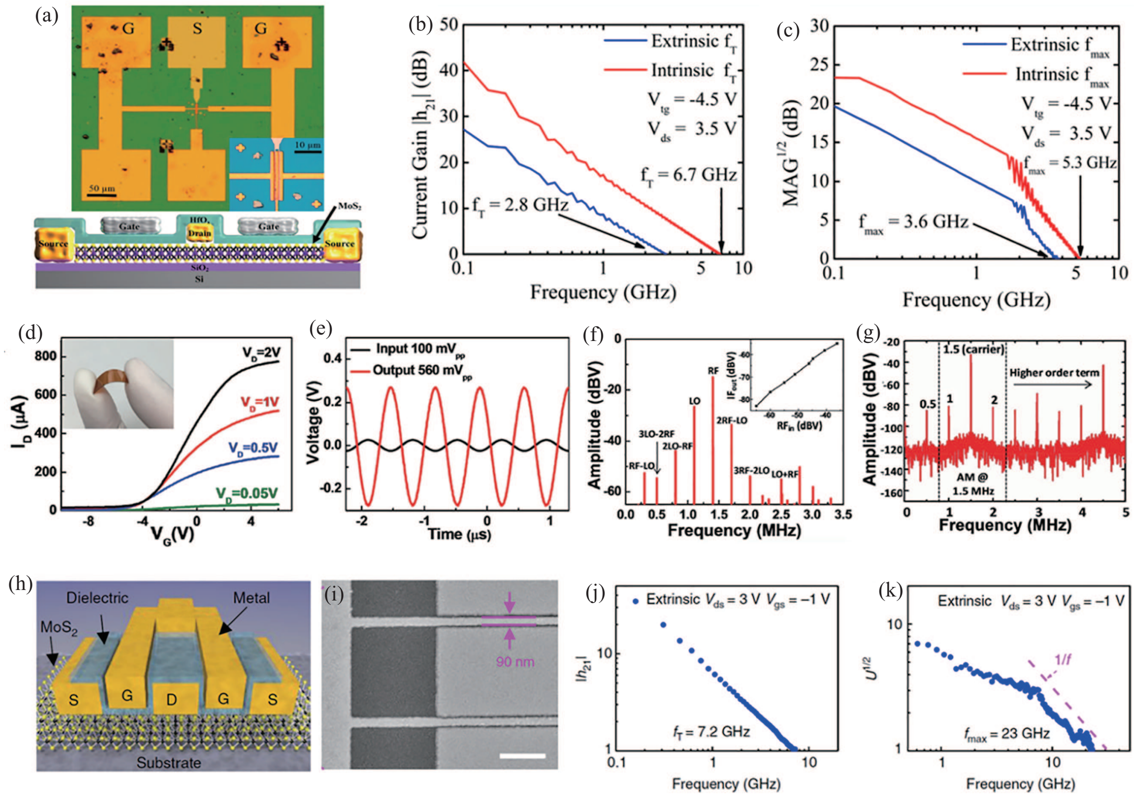

Figure 8 (Color online) (a) Optical image of the CVD MoS_2 in the ground-signal-ground structure (GSG). (b) Short circuit current gain $|h_{21}|$ versus frequency. (c) Maximum frequency of oscillation f_{max} versus frequency [119] @Copyright 2015 American Chemical Society. (d) Electrical characteristics of flexible MoS_2 FETs (L_g = 500 nm) at 300 K. Inset is an optical photograph of CVD MoS_2 FETs on the flexible substrate. (e) Input and output voltage waveforms of CS amplifier with a gain of 15 dB. The CS amplifier is based on MoS_2 flexible TFT ($f_{RF} \approx 1.4$ MHz). (f) Output frequency spectrum of MoS_2 FET-based RF mixer ($f_{RF} \approx 1.4$ MHz, $f_{LO} \approx 1.1$ MHz, $f_{IF} \approx 300$ kHz). The inset shows the conversion gain of the mixer is ca. −17 dB. (g) MoS_2 FET-based wireless AM (amplitude modulation) receiver output spectrum. The distance between transmit and receiver antenna is 5 m, and the carrier frequency (ω_C) is 1.5 MHz [120] @Copyright 2015 John Wiley and Sons. (h) Schematic illustration of bilayer MoS_2 RF transistor. (i) The SEM images of MoS_2 RF transistor with dual-channel structure scale bar is 500 nm. (j) Small-signal current gain $|h_{21}|$ versus frequency for device with gate length of 90 nm. (k) Unilateral power gain U versus frequency for device with gate length of 90 nm [121] @Copyright 2018 Springer Nature.

(1.5 MHz) and signals receive from an antenna, resulting in harmonic signals at the output.

Considering that bilayer MoS_2 films possess higher carrier mobility and higher density of states than monolayer, Gao et al. [121] performed a similar research on bilayer CVD-grown MoS_2 films. The schematic diagram of the bilayer MoS_2 RF transistor is illustrated in Figure 8(h). The SEM image (Figure 8(i)) shows excellent alignment of gate to source and drain. For the MoS_2 devices, the extrinsic cut-off frequency f_T and maximum oscillation frequency are respectively 7.2 GHz (Figure 8(j)) and 23 GHz (Figure 8(k)). Moreover, they demonstrated frequency mixer both on rigid and flexible substrate, which operated at 1.5 GHz, and it is the first time for CVD-grown MoS_2 based mixer to enter gigahertz regime.

7 Conclusion and outlook

Significant advances in 2D-TMDs have led to promising electronic and optoelectronic applications. Although most research progresses still occurred in research laboratories. The research direction has begun to translate from fundamental investigation into rudimentary functional circuits. Exploring synthesis methods to provide wafer-scale, continuous and uniform 2D-TMD film is still the main target in the near future, and integration technologies such engineering of doping, contact and interface of the TMD FETs also require more effort. Various improvements are needed for different circuit-level applications.

High mobility is needed for nearly all device applications; Precise control of doping and V_T is required for multi-level logic circuits; Achieving large ON/OFF current ratio and ideal subthreshold swing are required for low-power electronics; For optoelectronics, it is more important to enhance light absorption and improve fluorescence and electroluminescence quantum yields. Looking forward, all these still require the guidance from fundamental research to develop a comprehensive understanding of wafer-scale 2D-TMDs, and more collaboration between academic and industrial communities will bridge the gap between fundamental research and engineering applications.

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