

1

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U\_02power  
02power.SchDoc



U\_03config  
03config.SchDoc



U\_04fpga-io  
04fpga-io.SchDoc



U\_05fpga-pwr  
05fpga-pwr.SchDoc



U\_06ddr3  
06ddr3.SchDoc



U\_07connectors  
07connectors.SchDoc



# NeTV2 EVT2-A

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Title		
NeTV2 EVT2-A		
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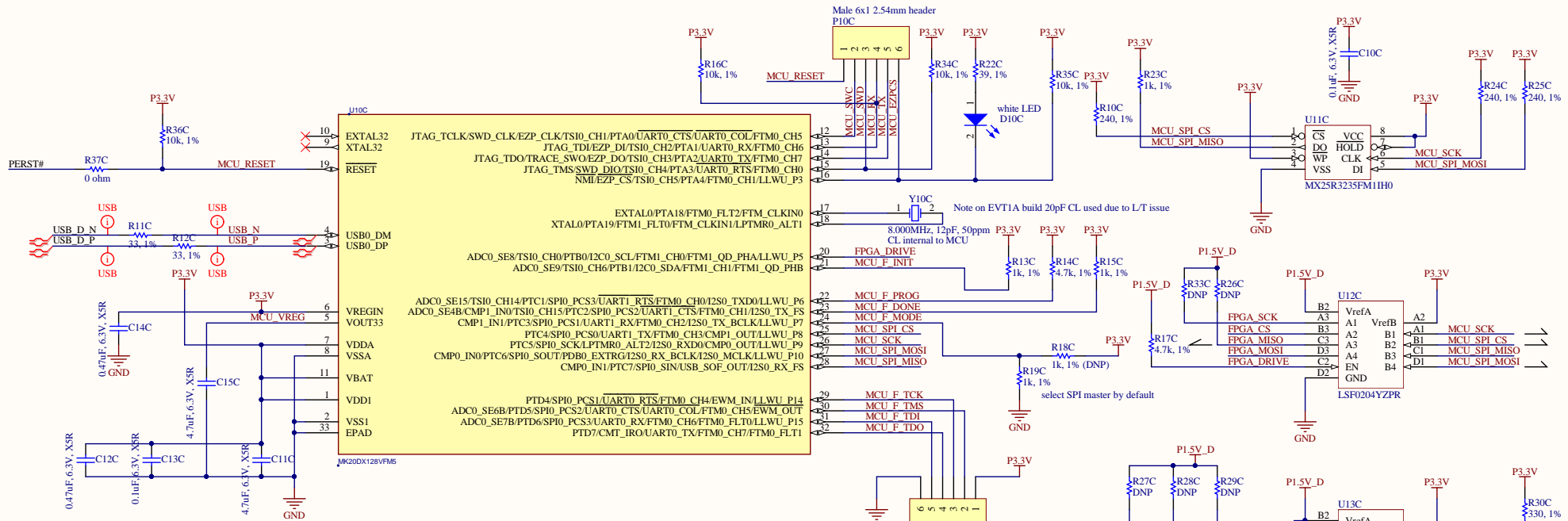
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#### Configuration plan:

1. CFGBVS on FPGA tied to 0V - VCCO\_0 set to 1.5V
2. MCU must initialize GPIOs within 5ms of power on.
3. MCU holds PROGRAM\_INIT low to hold off config
4. MCU selects SPI master mode for FPGA
5. MCU ensures FPGA\_DRIVE is asserted and it's SPI pins are tri-stated
6. MCU turns INIT into an input, allowing it to float
7. MCU pulses PROGRAM for 250ns minimum
8. MCU monitors DONE, reports status.

Note: MCU SPI pins remain Hi-Z at all times.  
FPGA configuration should succeed even when MCU is unprogrammed (but SPI is programmed) due to pull-up on FPGA\_DRIVE.

#### Update SPI ROM:

1. MCU disconnects FPGA by de-asserting FPGA\_DRIVE
2. MCU configures drive on SPI pins
3. Data arrives via USB and is written into SPI
4. MCU tri-states its SPI pins
5. MCU re-connects FPGA by asserting FPGA\_DRIVE
6. (optional) MCU initiates FPGA configuration by yanking PROGRAM

#### JTAG:

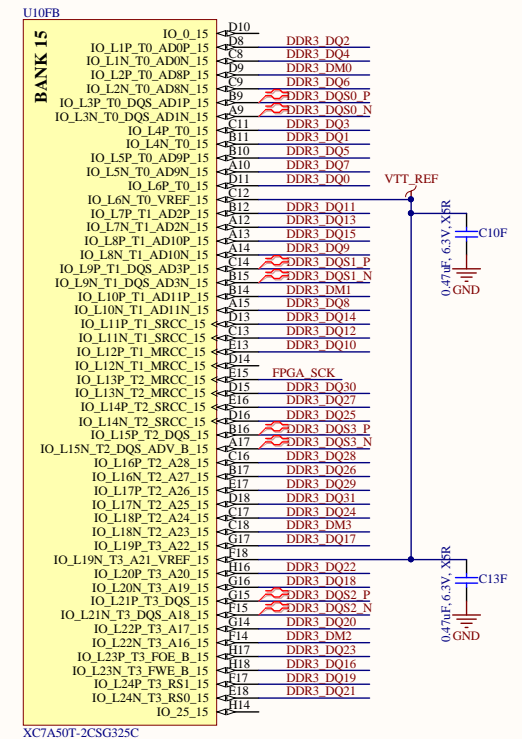
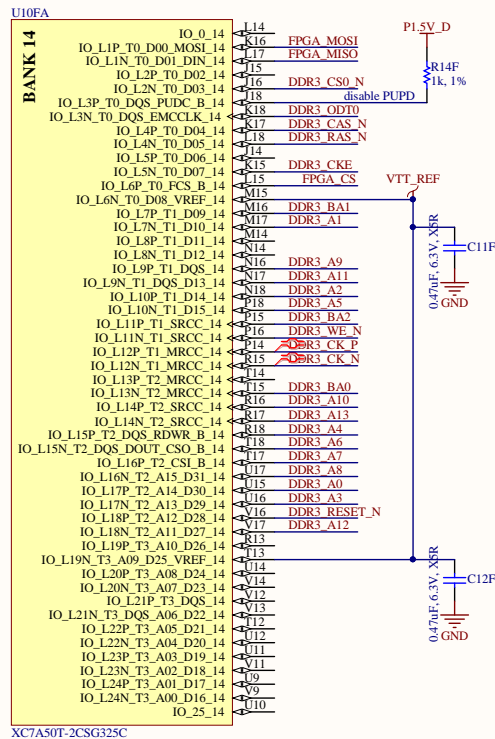
User must coordinate MCU pin state vs. optional external JTAG attachment.

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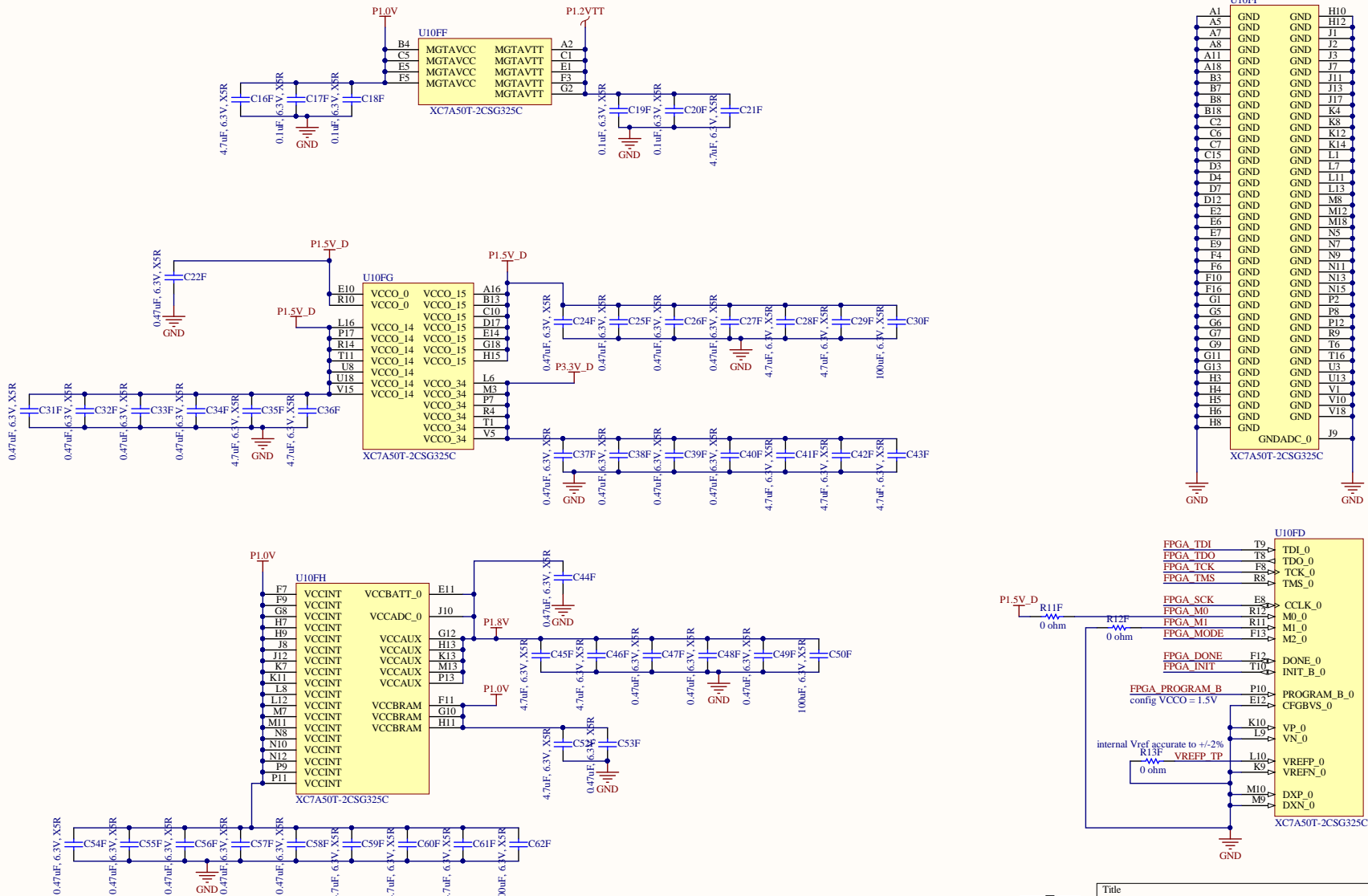
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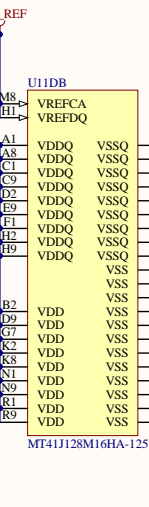
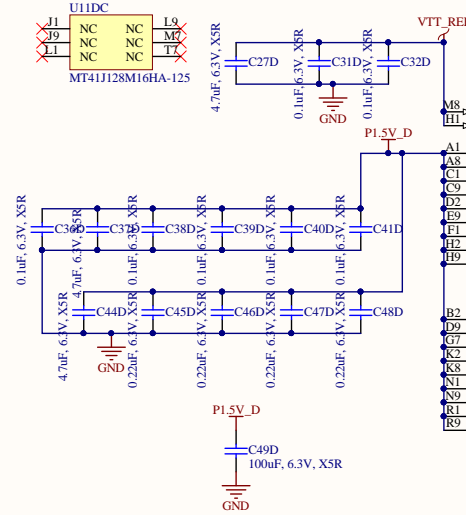
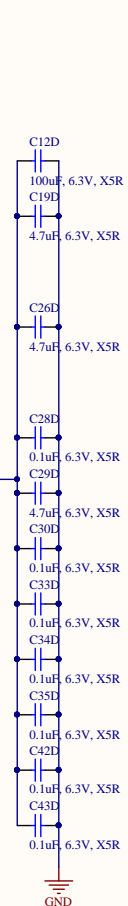
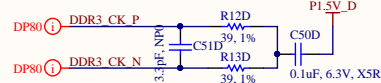
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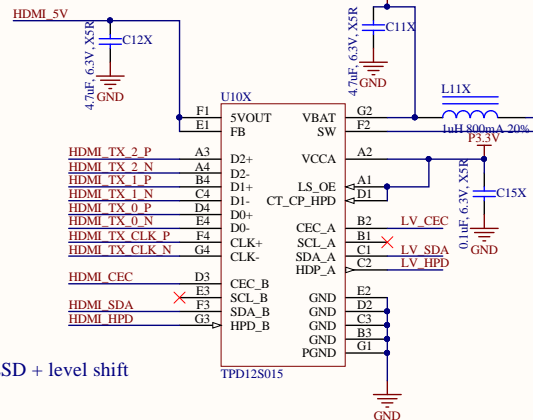
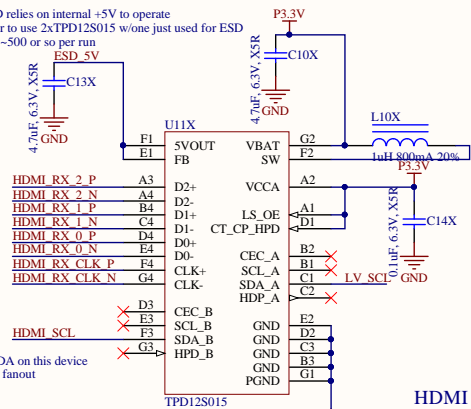
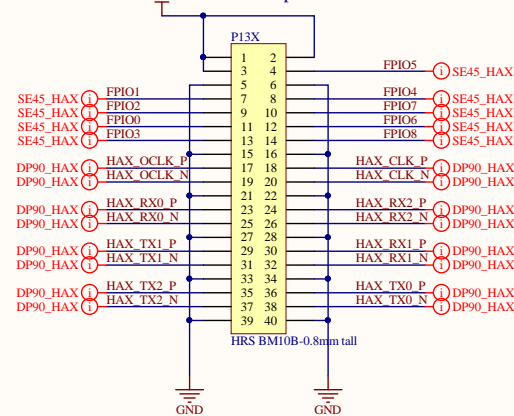
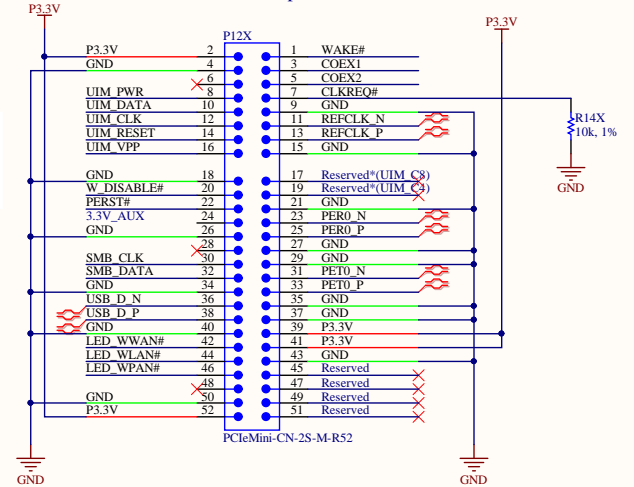
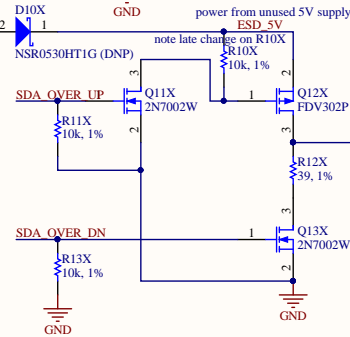
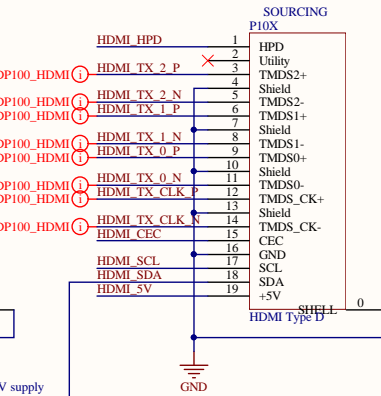
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