Hi3512 H.264 Encoding and Decoding Processor

Key Features

CPU Core
- ARM926EJ-S, 16 KB instruction cache, and 16 KB data cache
- Embedded close coupling memory with 2 KB instruction
- 32-bit RISC processor with the Harvard architecture
- Built-in MMU supporting various open operating systems
- Up to 288 MHz operating frequency

Video Encoding and Decoding
- H.264 Main Profile@Level3.0 encoding and decoding
- H.264 Baseline Profile@Level3.0 encoding and decoding
- MJPEG/JPEG Baseline encoding and decoding

Video Processing Performance
- Maximum codec performance is 90fps@D1 or 360fps@CIF.
- up to 3M pixels encoding performance with 5fps.
- The bit rate control mode with CBR and VBR.
- The bit rate range is between 32k bps and 20M bps.

Image Processing
- De-interlace pre-processing
- Video/Image scaling
- 4 areas front-end OSD
- 4 layers back-end OSD
- Contrast and saturation adjustment
- Video blocking of 4 areas
- Supporting the SAD/MV output at the macro block level and the flexible motion detection
- noise filter

Audio Encoding and Decoding
- Implementing various audio and voice encoding and decoding functions through the ARM core
- Up to 8 channels of real-time audio encoding and decoding
- 2-way audio

Security Engine
- Implementing various encryption/decryption algorithms such as AES, DES, and 3DES through the hardware
- Digital watermark technology

Video Interfaces
- Input
  - –2 channels of BT.656/601 YCrCb 4:2:2, 8 bits. Each interface supports two channels of BT.656 multiplex video input. SMPTE296M 720P, YC 4:2:2, 16 bits CCD and CMOS digital interfaces.
- Output
  - –1-channel BT.656 interface.

Audio Interfaces
- I2S x 2
  - –8 bits, 16 bits or 32 bits
  - –\Sample frequency of 4–48 kHz.

Peripheral Interfaces
- PCI V2.3
  - –Compatible with the miniPCI
  - –Supporting the master and slave modes
- UART x 3
- IR
- I2C
- SPI, master and slave modes
- GPIO
- SDIO 2.0
- USB 1.1 Host
- USB 2.0 OTG
- MII interface ,10/100Mbit/s duplex
- RTC, independent supply power

Memory Interface
- DDR2 SDRAM interface
  - –16 bits or 32 bits
  - –Up to 512 MB
- NOR flash interface
  - –8 bits
  - –2 banks, each up to 32 MB

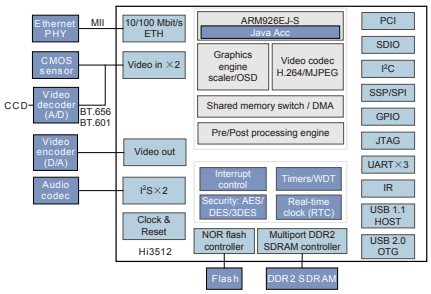
SDK
- Linux-based SDK
- High-performance H.264 PC decoding library

Power Consumption
- 600 mW typical power consumption
- Multiple levels of power-down modes

Operating voltage
- 1.2 V for core
- 3.3 V for IO with 5 V tolerance
- 1.8 V for DDR2 DRAM I/O

Package
- 441-pin TFBGA
- 19 mm x 19 mm, 0.8-mm ball pitch

Functional Block Diagram



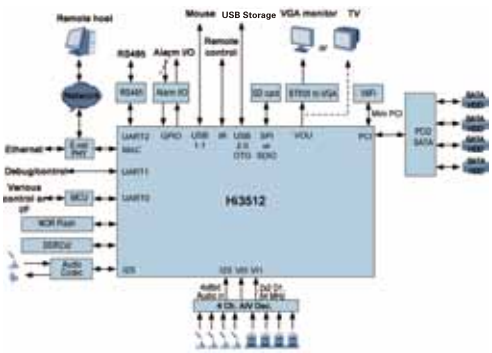
The Hi3512 is a high-performance communications media processor based on the ARM9 processor core and the video hardware acceleration engine. The Hi3512 is highly integrated and programmable and supports multiple protocols such as H.264 and MJPEG. It is used in various fields such as the real-time video communication and the digital video monitoring. The video processing unit of the Hi3512 supports various real-time encoding and decoding protocols such as H.264 Main/Baseline Profile, MJPEG, and JPEG. It also supports that the H.264 encoding and decoding operations (with 30fps@D1 frame rate) are performed simultaneously. In addition, up to 3-mega-pixel encoding is supported for the MJEPG and JPEG formats. The powerful encoding algorithm of the H.264 MainProfile greatly improves the video quality and provides the field encoding or the frame encoding flexibly to adapt to different display terminals of clients. The video processing unit of the Hi3512 also supports the encoding of two channels of stream (H.264/MJPEG).

The image processing unit of the Hi3512 provides functions such as the De-interlace algorithm processing and the flexible movement detection and supports the video/image scaling and the OSD.

Application Fields and Typical Application Scenarios

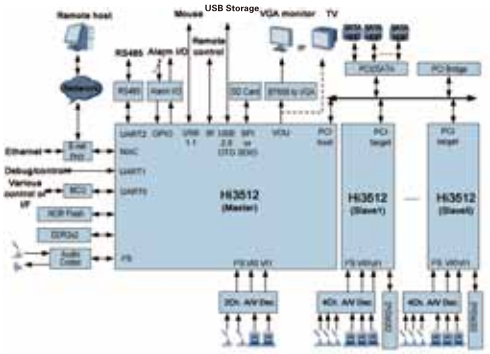
- Digital video server
- Digital video recorder
- Video Compression Card

4-Channel CIF DVR Board with a Single Hi3512



4–16 Channels D1 DVR Board with 2–6 Hi3512s

2 chips for 4-channel D1 DVR
3 chips for 8-channel D1 DVR
6 chips for 16-channel D1 DVR (an independent CPU is recommended in the solution)



HD IP Camera Board with a Single Hi3512