23rd IEEE International Conference on High Performance Computing

Hyderabad, India • December 19-22, 2016

PROGRAM OVERVIEW

Starting on Monday, December 19th, the first day of HiPC 2016 features four workshops and concludes with an Industry Gala. The technical program on Days 2, 3 and 4 will showcase three keynote speakers and seven single track sessions of forty peer reviewed papers from all over the world covering important and timely topics in all areas of high performance computing, data, and analytics. On Days 2 and 3, there will be a full program of industry exhibits and related events including Industry, Research and Users Symposium (IRUS) sessions to provide a forum for presenting state-of-the-art in HPC platforms and technologies, discussing best practices, and exchanging experiences. In addition, industry representatives will host BoF sessions on these two days. On Days 2 and 3, posters of work selected for the Student Research Symposium will be on display, and the conference will host the Intel and NVIDIA sponsored Student Parallel Programming Challenges. Wednesday evening's Conference Banquet will feature a special cultural program.

KEYNOTE SPEAKERS

Tuesday, December 20th – Day 2 Keynote

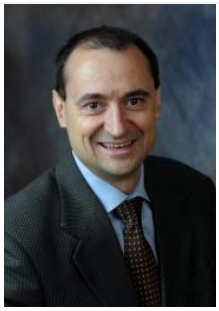
Genomes Galore: Big Data Challenges in the Life Sciences

Srinivas Aluru
Professor, School of Computational Science and Engineering, Georgia Institute of Technology, USA

Wednesday, December 21st – Day 3 Keynote

China's HPC development in the next 5 years

Depei Qian
Dean of the School of Data and Computer Science
Sun Yat-sen University, China



Thursday, December 22nd – Day 4 Keynote

Toward Extreme-Scale Processor Chips

Josep Torrellas
Saburo Muroga Professor of Computer Science, University of Illinois Urbana-Champaign

TECHNICAL PROGRAM

The HiPC 2016 technical program on Days 2, 3 and 4 will consist of 40 peer reviewed papers chosen from nearly 200 submissions from all over the world. The papers will be presented in seven single-track sessions and will cover important and timely topics in all areas of high performance computing. The three keynote speakers will open the morning plenary sessions.

WORKSHOPS

Four workshops covering diverse topics complementary to the conference technical program will be held on Day 1 of the conference. The BIGDF and CFD workshops will be full day events, and workshops 3 and 4 have been shaped as half-day events.

1. Foundations of Big Data Computing (BiGDF)
2. Computational Fluid Dynamics (CFD)
3. High Performance Computing and Big Data in Molecular Engineering (HBME)
4. Software Composable Infrastructure (SCI)

Peer reviewed papers selected for presentation in Workshops 1, 2 and 3 are included in the proceedings, and abstracts for presentations in Workshop 3 are also part of the proceedings to be distributed at the conference. Abstracts for keynote speakers in each workshop are included in the Workshop Introduction file in the proceedings as well as the individual webpages for the workshops.

STUDENT RESEARCH SYMPOSIUM

The 9th HiPC Student Research Symposium is aimed at stimulating and fostering student research, and providing an international forum to highlight student research accomplishments in HPC. The symposium also gives students exposure to the best practices of senior HPC researchers in academia and industry. In a departure from previous years, the 2016 symposium will feature only student posters - there will be no talks by students – and the posters will be on display on both Day 2 and Day 3 of the conference, next to industry exhibits. Student authors will be available during breaks to answer questions and during a dedicated session on Wednesday afternoon.

ACADEMIC BoF SESSIONS

HiPC introduced this format in 2014 with the purpose of fostering greater participation by the academic community at HiPC, including both domestic and international representation. With a focus on emerging areas of interest, the goal is to stimulate new research ideas, address specific problems, and build a research community. This year to be held on Day 2, there will one ABoF with the topic of Education in Parallel and Distributed Computing.

INDUSTRY EVENTS

The conference welcomes (and strongly encourages) industry participation on all days at all levels including in the technical program and student symposium. The industry/research exhibition, to be held on December 20th and 21st, will include booths and demonstrations and will showcase products, services and current work from vendor companies and R&D laboratories. **Two Industry, Research and Users Symposium (IRUS) sessions** on the topics of HPC Data Management Challenges and Advances in Applied Machine Learning and Analytics will be held on Days 2 and 3 and will bring together solution providers and users of HPC in a forum to discuss platforms and technologies and best practices. **Industry supporting sponsors will host three BoF's** also on Day 2.

HiPC 2016 PROGRAM DAILY SCHEDULE

Please check the Mobile App and postings at the venue for up-to-date information on locations and schedules for each event. The following shows time and location for all events.

Day	Start Time	End Time	Event	HICC Room
Mon			*Breakfast @ 7:30 – Lunch @ 1:00*	Atrium-Foyer Ground Floor
Mon			*Breaks: Morning Break@ 10:30 – Afternoon @ 4:00*	Atrium-Foyer Ground Floor
Mon	8:30 AM	6:30 PM	Industry Exhibit Booth Set-up	MR G.03+G.04+G.05+G.06
Mon	8:30 AM	6:30 PM	**Workshop 1: BIGDF**	Hall 1
Mon	8:30 AM	4:00 PM	**Workshop 2: CFD**	MR G.01
Mon	8:30 AM	1:00 PM	**Workshop 4: SCI**	Hall 2
Mon	2:00 PM	6:30 PM	**Workshop 3: HBME**	Hall 2
Mon	4:30 PM	6:30 PM	SRS Poster Set-up	MR G.01+G.02
Mon	6:30 PM	8:00 PM	**Plenary Industry Gala Opening & SRS Posters**	MR G.01 - MR G.06 + Foyer
Tue			*Breakfast @ 7:00 – Lunch @ 12:00*	Atrium-Foyer Ground Floor
Tue			*Breaks: Morning Break@ 9:30 – Afternoon @ 3:00*	Atrium-Foyer Ground Floor
Tue	8:00 AM	8:30 AM	**Plenary HiPC 2016 Inauguration**	Halls 1 & 2
Tue	8:30 AM	9:30 AM	**Keynote Talk 1: Srinivas Aluru**	Halls 1 & 2
Tue	10:00 AM	12:00 PM	**TechSession 1: Applications**	Halls 1 & 2
Tue	10:00 AM	12:00 PM	**IRUS Session 1: HPC Data Management Challenges**	MR 1.05
Tue	10:00 AM	12:00 PM	**NVIDIA BoF Session**	MR 1.06
Tue	10:00 AM	5:30 PM	SRS Posters on display	MR G.01+G.02
Tue	10:00 AM	5:30 PM	Industry Demos & Exhibits	MR G.03+G.04+G.05+G.06
Tue	1:00 PM	3:00 PM	**TechSession 2: Algorithms for data and data management**	Halls 1 & 2
Tue	1:00 PM	3:00 PM	**Academic BoF Session: Education in PDC**	MR 1.05
Tue	1:00 PM	3:00 PM	**Intel BoF**	MR 1.06
Tue	3:30 PM	5:30 PM	**TechSession 3: Memory and I/O**	Halls 1 & 2
Tue	3:30 PM	5:30 PM	**Programming Contest**	MR 1.05
Tue	3:30 PM	5:30 PM	**Mellanox BoF Session**	MR 1.06
Wed			*Breakfast @ 7:30 – Lunch @ 12:00*	Atrium-Foyer Ground Floor
Wed			*Breaks: Morning Break@ 9:30 – Afternoon @ 3:00*	Atrium-Foyer Ground Floor
Wed	8:30 AM	9:30 AM	**Keynote Talk 2: Depei Qian**	Halls 1 & 2
Wed	10:00 AM	12:00 PM	**TechSession 4: Numerical applications**	Halls 1 & 2
Wed	10:00 AM	12:00 PM	**IRUS Session 2: Advances in Applied Machine Learning and Analytics**	MR 1.05
Wed	10:00 AM	5:30 PM	SRS Posters on display	MR G.01+G.02
Wed	10:00 AM	5:30 PM	Industry Demos & Exhibits	MR G.03+G.04+G.05+G.06
Wed	7:30 AM	8:30 AM	*Sponsor Feedback Breakfast (by invitation)*	MR 1.06
Wed	12:00 PM	1:00 PM	*Sponsor Feedback Lunch (by invitation)*	MR 1.06
Wed	1:00 PM	3:00 PM	**TechSession 5: Resilience and compilers**	Halls 1 & 2
Wed	3:30 PM	5:30 PM	**SRS Posters – Student authors available**	MR G.01+G.02
Wed	6:30 PM	9:30 PM	**Awards, Cultural Programme, Banquet**	Halls 1 & 2
Thu			*Breakfast @ 7:30 – Lunch @ 12:00*	Atrium-Foyer Ground Floor
Thu			*Morning Break@ 9:30*	Atrium-Foyer Ground Floor
Thu	8:30 AM	9:30 AM	**Keynote Talk 3: Josep Torrellas**	Halls 1 & 2
Thu	10:00 AM	12:00 PM	**TechSession 6: Parallel algorithms**	Halls 1 & 2
Thu	1:00 PM	3:00 PM	**TechSession 7: Software architecture**	Halls 1 & 2

See maps of venue in the mobile app.

Day 1 - Monday, December 19

Breakfast @ 7:30, Breaks @ 10:30 and 4:00, Lunch @ 1:00

HiPC 2016 WORKSHOP 1:
Foundations of Big Data Computing (BIGDF)

8:50-10:30 BIGDF Session 1
Opening Remarks by Workshop Chairs

QoS aware Resource Management for Apache Cassandra
Yasaswi Kishore, Venkat Datta, KV Subramaniam, Dinkar Sitaram

A High Performance Computing Framework for Data Mining
Navneet Goyal, Sundar Balasubramaniam, Poonam Goyal, Saiyedul Islam, Mohit Sati

Application of an Asset Bubble Model to Microblog Data Analytics
K. M. George, Ashwin Kumar Thandapani Kumarasamy

11:00-1:00 BIGDF Session 2

Keynote Address 1: "A Framework for Real-Time Event Detection for Emergency Situations using Social Media Streams"
Prof. Vijay V. Raghavan, Alfred and Helen Lamson Endowed Professor in Computer Science, Center for Advanced Computer Studies, University of Louisiana, U.S.A.

A fast, Apriori based approach to Association Rule Mining in large and growing datasets
Atmika Honnalgere, Abhinav Patluri

A Hybrid Recommender System using Weighted Ensemble Similarity Metrics and Digital Filters
Ramesh Naidu Laveti, Janaki Ch, Supriya N Pal, N. Sarat Chandra Babu

2:00-4:00 BIGDF Session 3

Keynote Address 2: "Big Data and High Performance Computing: Convergence?"
Prof. Geoffrey Fox, Distinguished Professor, School of Informatics and Computing, Indiana University, Bloomington, Indiana, USA

High Frequency Trading with Complex Event Processing
Ajay Acharya, Nandini Sidnal

Big Data Analytics Architecture for Agro Advisory System
Purnima Shah, Deepak Hiremath, Sanjay R Chaudhary

4:30-6:00 BIGDF Session 4

#ChennaiFloods: Leveraging Human and Machine Learning for Crisis Mapping during Disasters using Social Media
Bhuvaneswari Anbalagan, Valliyammai Chinnaiah

Multi-Dimensional Predictive Analytics for Risk Estimation of Extreme Events
Laks Raghupathi, David Randell, Emma Ross, Kevin C. Ewans, Philip Jonathan

Compression acceleration using GPGPU
Krishnaprasad Shastry, Avinash Pandey, Ashutosh Agrawal, Ravi Sarveswara

HiPC 2016 WORKSHOP 2:
Computational Fluid Dynamics (CFD)

8:30-10:30 CFD Session 1
Opening of CFD Workshop

Keynote: Using High Performance Computing (HPC) for understanding Fluid Flows
Speaker: Prof. Sanjay Mittal, Aerospace Engineering, IIT Kanpur

An efficient GPU parallelization for arbitrary collocated polyhedral finite volume grids and its application to incompressible fluid flows
Presenter: Shashank Jaiswal, Indian Institute of Technology Hyderabad

Sub cooled boiling: validation by using different CFD models
Authors: Venkateswara Sontireddy and Sridhar Hari, CD-Adapco

11:00–1:00 CFD Session 2

Improvements in Free Surface Flow Numerics using Coupled VOF and Pseudo Transient Solver
Authors: Vinay Gupta, Kvss Srikanth, and Hemant Punekar, ANSYS Software Pvt. Ltd.

An object oriented parallel finite element scheme for computations of PDEs: Design and implementation
Authors: Sashikumaar Ganesan, Raviteja Meesala, and Abdus Shamim, Indian Institute of Science

Importance of Bubble size distribution in Gas-Liquid Flows
Authors: Ravindra Aglave and Thomas Eppinger, CD-Adapco

A Numerical Investigation on bubble formation in Coolant channel with various Ethylene Glycol and water compositions and change in contact angle
Authors: Vamshi Krishna Chitikase and Chih-Cheng Hsu, GM

2:00-4:00 CDF Session 3 Invited Speakers & Panel Discussion (details to be announced)

HiPC 2015 WORKSHOP 3:
High Performance Computing and Big Data in Molecular Engineering (HBME)

2:00-4:00 HBME Session 1 (Chair: J. K. Singh)
Keynote: Transitions to and from jammed states in glasses and sphere packings under shear deformation.
Speaker: Prof. S. Sastry, JNCASR, Bengaluru

Paper: Towards understanding optimal load balancing of heterogeneous short-range molecular dynamics
Presenter: S. Hirschmann, D. Pflüger, C. W. Glass

Abstract: Molecular dynamics simulation of nanoscopic Couette flow and lubricated nano-indentation
S. Stephan, M. P. Lautenschläger, M. T. Horsch, H. Hasse

4:40-6:05 HBME Session 2 (Chair: C. W. Glass)

Abstract: In-silico skin model: A tool for virtual testing of formulations
R. Gupta, B. S. Dwadasi, B. Rai

Abstract: Insight into the nature of evaporation processes enabled by massively parallel molecular dynamics simulations, M. Heinen, R. S. Chatwell, J. Vrabec

Abstract: Round robin study of molecular simulation programs, M. Schappals, H. Hasse

HiPC 2016 WORKSHOP 4:
Software Composable Infrastructure (SCI)

(This workshop has talks only; no papers or abstracts are included in proceedings.)

09:00 –10:30 SCI Session 1

Title: Composable Pooled systems with Intel Rackscale Design
Speaker: Mrittika Ganguli, Intel

Title: Software-Defined Environments for Science
Speaker: Manish Parashar, Rutgers University

11:00 – 12:45 SCI Session 2

Title: Event Digest for Hyperscale data center telemetry
Authors: Ananth S. Narayan and Lucasz Grzymkowski, Intel

Title: Applying the ideas of NFV and SDN to Telecom Networks
Speaker: Mythili Vutukuru, Indian Institute of Technology Bombay

Title: Rack scale architecture Challenges and Opportunities
Speaker: Chakri Padala, Ericsson

Student Research Symposium (SRS)

Starts at 6:30 PM – Monday, December 19th

The following papers have been accepted for poster presentation on both Day 2 and Day 3 of the conference. They will be on display next to the conference industry exhibits, and available for viewing throughout both days. Student authors will be available during breaks to answer questions, and there will be a dedicated session on Wednesday afternoon.

Design and Implementation of Generative Models for Odor Classification Using Electronic Nose.
Kumar Shashvat and Amol Bhondekar

Scheduling of Cholesky Factorization with lookahead information.
Suraj Kumar, Olivier Beaumont and Lionel Eyraud-Dubois

Implementing Deep v-support vector machine for classification problem in spark cluster.
Sekhar Banarjee and Motahar Reza

Data Cube 2.0: Data Dodecahedron(DRON) Operator using Euclid's Model for OLAPing BIGDATA Aggregation.
Sharath Yaji and Neelima Bayyapu

Branch Predictor Attacks : An Empirical Exploration.
Moumita Das and Arnab Kar

CoKeeper: An Adaptive Co-resident VM Membership Maintenance Method.
Ziqi You, Yi Ren, Renshi Liu, Jianbo Guan and Yusong Tan

Fast Large Graph Algorithms on GPU.
Ankur Anandapu and Basavaraj Talawar

Accelerated Fluid Simulation of Low Temperature Plasmas on Intel Xeon Phi MIC Architecture.
Henil Shah, Anurag Gupta, Saumya Bhadani and Bhaskar Chaudhury

HBaseChainDB – Blockchain Infrastructure for the Hadoop Ecosystem over HBase.
Adarsh Saraf, Sanju Singh, Naveen H. and Pallav Kumar Baruah

Scalable I/O Management in Multi-tenant Hadoop Clusters.
Amrit Kumar, Sanik Thapa, Shubhranshu S. Panda and Pallav Kumar Baruah

A Scalable Vertex Centric Distributed Algorithm for Streaming Betweenness Centrality.
Sai Ganesh Muthuraman, Yogesh Murthy K, Bala Praveen Kumar and Pallav Kumar Baruah

Single Image Super Resolution using Transformed Self-Exemplars:A Heterogeneous Parallel Computing Approach.
Chaitanya Pavan Tanay Kondapalli, Diwakar Kartheek Pingali, Jyothi Kumar Behara, Pallav Kumar Baruah, Chandrasekaran Venkatachalam and Srikanth Khanna

EFOCS: An Efficient and Fast Overlapped Community Detection System For Complex Networks.
Mrudula Sarvabhatla and Chandra Sekhar

Traffic big data prediction and visualization using Decision Forest Regression Algorithm.
Lakshmi Singh, Rajat K Pathak and Motahar Reza

Distributed Algorithms for Subgraph-Centric Graph Platforms.
Diptanshu Kakwani and Yogesh Simmhan

Partitioning Test Cases for Heap Programs.
Awanish Pandey and Subhajit Roy

Block Placement Strategy and Handling Small Files Problem in Heterogeneous Hadoop Cluster.
Ch.Bhaskar Vishnuvardhan and Pallav Kumar Baruah

Multi-GPU Graph Traversal with Unified Virtual Memory.
Vamsi Bokam and Rupesh Nasre

An Evolutionary Algorithm for Virtual Machine Placement in Cloud Environment.
Wahdat Safia, Nirbhay Chandorkar, Kumar Vaibhav, Anup Bhattacharjee and Rajesh Kalmady

ARM Wrestling with x64: A Study of Web and Terasort Workloads.
Sarthak Sharma and Yogesh Simmhan

Streaming String Sort : A Hybrid String Sort on CPU+GPU.
Kalpit Thakkar and P J Narayanan

On-Chip Network simulation acceleration using FPGAs.
Khyamling Parane, Prabhu Prasad B M and Basavaraj Talawar

HiMesh : A Low Power High Performance Improved Architecture for 3-D On-Chip Networks.
Anagh Singh, Anamik Sarvaiya and Basavaraj Talawar

Texturizing PPCG: Supporting Texture Memory in a Polyhedral Compiler.
Abhishek Patwardhan and Ramakrishna Upadrasta

Customized Face Classification to Reduce the Training Time: A Proposal.
Raghurama Rao, Gururaja Rao, Rajesh Poojary, Gajendra S Patagara and Neelima B

A Data Locality based MapReduce Scheduler in Heterogeneous Environments.
Nenavath Srinivas Naik, Atul Negi and Sastry Vinjamuri N

A Comparative Study of Vectorization in Compilers.
Das Santanu, Dangeti Tharun Kumar, Bora Utpal and U Ramakrishna

A Clustering-Based Approach for Workload Estimation in the Cloud.
Vasu Jindal

An Analysis of Cache Restoration Prefetching Techniques for Addressing the Cold Cache Problem.
Nagakishore Jammula

Resource Allocation and Placement for Distributed Stream Processing.
Aakash Khochare and Yogesh Simmhan

6:30 PM – 8:00 PM Monday, December 19
Plenary Industry Gala Opening: Exhibits & SRS Posters

Starts at 6:30 PM Monday, December 19 10:00 AM – 5:30 PM Tuesday, December 20 and Wednesday, December 21
Industry/Research Exhibition
Below are the companies who will be providing exhibits and demonstrations at HiPC 2016. Attendees are invited to visit booths and check posted schedules for demonstrations and talks and collect materials these exhibitors have prepared for the conference. **Acer** **Avnet** **BOSTON** **Cray** **Google** **G.T. Enterprise** **IEEE Standards Association** **Infosys** **Intel** **Mellanox** **Microsoft** **NetApp** **Netweb** **Nvidia** **SanDisk** **Shell** **Xilinx**

Day 2 - Tuesday, December 20

Breakfast @ 7:00, Breaks @ 9:30 and 3:00, Lunch @ 12:00 (1 hour)

8:00 AM – 8:30 AM Tuesday, December 20th

Plenary Session: Conference Inauguration and Opening Remarks

8:30 AM – 9:30 AM

HiPC 2016 Keynote Presentation 1
Session Chair: Pavan Balaji

Genomes Galore: Big Data Challenges in the Life Sciences
Srinivas Aluru
School of Computational Science and Engineering, Georgia Institute of Technology, USA

Abstract: While the big data revolution in the consumer, business, and social networks domains is widely known, a similar revolution is taking place in the sciences and engineering driven by high-throughput instrumentation. This talk will feature big data challenges in the life sciences, primarily due to advances in sequencing that resulted in several orders of magnitude throughput increases per unit cost during the last decade. These advances are democratizing big data generation capabilities and spawning new scientific inquiries that would not be feasible otherwise. The time, cost, and complexity of data analysis have overtaken the cost and speed of data generation as the primary bottlenecks, posing significant challenges for computer scientists. I will present an overview of my group's research in addressing some of these issues through the development of parallel algorithms and high performance computing approaches. Apart from opening new avenues of investigation in parallel processing, research in this domain is also leading to broadly applicable techniques in areas such as graph analytics and parallel machine learning. I will also brief the audience on the ongoing federal initiatives in the United States aimed at nurturing multi-stakeholder partnerships to advance such big data challenges.

10:00 AM – 12:00 PM Tuesday, December 20

Technical Session 1: Applications
Session Chair: Suren Byna

Soft Error Detection for Iterative Applications Using Offline Training
Jiaqi Liu and Gagan Agrawal (Ohio State University, USA)

Fault Tolerant Frequent Pattern Mining
Sameh Shohdy (The Ohio State University, USA); Abhinav Vishnu (Pacific Northwest National Laboratory, USA); Gagan Agrawal (The Ohio State University, USA)

Parallel Performance-Energy Predictive Modeling of Browsers: Case Study of Servo
Rohit Zambre (University of California, Irvine, USA); Lars Bergstrom (Mozilla Research, USA); Laleh Aghababaie Beni and Aparna Chandramowlishwaran (University of California, Irvine, USA)

Optimization of Brain Mobile Interface Applications Using IoT
Koosha Sadeghi, Ayan Banerjee, Javad Sohankar and Sandeep K.S. Gupta (Arizona State University, USA)

Mizan-RMA: Accelerating Mizan Graph Processing Framework with MPI RMA
Mingzhe Li, Xiaoyi Lu, Khaled Hamidouche, Jie Zhang and Dhabaleswar K. (DK) Panda (The Ohio State University, USA)

CUDA M3: Designing Efficient CUDA Managed Memory-aware MPI by Exploiting GDR and IPC
Khaled Hamidouche, Ammar Ahmad Awan, Akshay Venkatesh, and Dhabaleswar K. (DK) Panda (The Ohio State University, USA)

10:00 AM – 12:00 PM Tuesday, December 20

IRUS 1: HPC Data Management Challenges

Pulipati Madhav, CEO - Photonics Valley Corporation, Government of Telangana
Topic: Photonics

Jean-Thomas Acquaviva, Data Direct Networks, France
Topic: Understanding Exascale HPC Applications with I/O Profiling

Kalyana Chadalavada, Intel
Topic: Exascale I/O Systems

P Shasidhar Reddy, National Remote Sensing Centre, ISRO
Topic: Data Management for Satellite Data Platform

10:00 AM – 12:00 PM Tuesday, December 20

NVIDIA BoF Session

Faculty Discussion, Innovation Awards Presentation and Academic Program Update

Speaker:
Ganesh Mahabala, India Academic Program Head

1:00 PM – 3:00 PM Tuesday, December 20

Technical Session 2: Algorithms for data and data management
Session Chair: Gagan Agrawal

Parallel Implementation of Lossy Data Compression for Temporal Data Sets
Zheng Yuan (Northwestern University, USA); William Hendrix (University of South Florida, USA); Seung Woo Son (University of Massachusetts Lowell, USA); Christoph Federrath (Australian National University, Australia); Ankit Agrawal, Wei-keng Liao and Alok Choudhary (Northwestern University, USA)

Scalable Parallel Algorithms for Shared Nearest Neighbor Clustering
Sonal Kumari, Saurabh Maurya, Poonam Goyal, Sundar S. Balasubramaniam, and Navneet Goyal (BITS-Pilani, India)

DCRoute: Speeding up Inter-Datacenter Traffic Allocation while Guaranteeing Deadlines
Mohammad Noormohammadpour and Cauligi Raghavendra (University of Southern California, USA); Sriram Rao (Microsoft, USA)

Efficient Data Redistribution to Speedup Big Data Analytics in Large Systems
Long Cheng (Eindhoven University of Technology, The Netherlands); Tao Li (TU Dresden, Germany)

Load Balancing for Molecular Dynamics Simulations on Heterogeneous Architectures
Steffen Seckler, Nikola Tchipev, Hans-Joachim Bungartz and Philipp Neumann (Technical University of Munich, Germany)

1:00 PM – 3:00 PM Tuesday, December 20

Academic BoF: Education in Parallel and Distributed Computing

The session will be organized to include brief talks from Early Adopter Awardees and to discuss best practices and experiences of the early adopters in their country and also recommend action points and suggestions that can be incorporated by the participants in their respective institutions. The session will provide an open discussion forum to address participant questions such as the nature and availability of resources for teaching the intended topics and the suggested mechanisms to incorporate these topics in the teaching plan without sacrificing material on traditional core topics.

Organizers:

- Kishore Kothapalli, IIIT Hyderabad
- R. Govindarajan, IISc, Bengaluru

1:00 PM – 3:00 PM Tuesday, December 20

Intel BoF Session

Next generation Intel solutions for High Performance Computing

Compute: Knights Landing, FPGA, Skylake
- Speaker: Seetha Rama Krishna Nookala

Storage and Interconnect: 3DX Point, IEEL, OPA Integration
- Speaker: Paresh Pattani

Software: Orchestrator, Next generation Intel tools
- Speakers: Chakravarthy Nagarajan and Austin Cherian

3:30 PM – 5:30 PM Tuesday, December 20

Technical Session 3: Memory and I/O
Session Chair: Ashok Srinivasan

MEC: The Memory Elasticity Controller
Roberto Sawamura, Cristina Boeres and Vinod E.F. Rebello (Universidade Federal Fluminense, Brazil)

Phoenix: Memory Speed HPC I/O with NVM
Pradeep Fernando, Sudarsun Kannan, Ada Gavrilovska and Karsten Schwan (Georgia Institute of Technology, USA)

Dynamic Data Layout Optimization for High Performance Parallel I/O
Everett Neil Rush, Bryan Harris and Nihat Altiparmak (University of Louisville, USA); Ali Saman Tosun (University of Texas at San Antonio, USA)

Read Consistency in Distributed Database Based on DMVCC
Jie Shao (Tsinghua University and Baidu, Inc,, P.R. China); Boxue Yin, Bujiao Chen, Guangshu Wang, Lin Yang, Jianliang Yan and Jianying Wang (Baidu, Inc,, P.R. China); Weidong Liu (Tsinghua University, P.R. China)

Data Elevator: Low-contention Data Movement in Hierarchical Storage System
Bin Dong, Suren Byna, Kesheng Wu, Prabhat, Hans Johansen, Jeffrey N. Johnson, and Noel Keen (Lawrence Berkeley National Laboratory, USA)

Telescoping Architectures: Evaluating Next-Generation Heterogeneous Computing
Konstantinos Krommydas and Wu-chun Feng (Virginia Tech, USA)

3:30 PM – 5:30 PM Tuesday, December 20

Programming Contest

Poster boards for the programming contest, sponsored by Nvidia and Intel, will be displayed as part of the SRS poster session starting Monday evening. There will be six posters in total, including the top three winners from each track. On Tuesday, there will be a special program as follows:

3:30 PM to 3:40 PM	Welcome and Session Introduction
3:40 PM to 4:00 PM	Nvidia track winner presentation
4:00 PM to 4:20 PM	Intel track winner presentation
4:20 PM to 4:50 PM	Presentation from Nvidia
4:50 PM to 5:20 PM	Presentation from Intel
5:20 PM to 5:30 PM	Closing

3:30 PM – 5:30 PM Tuesday, December 20

Mellanox BoF Session

Breaking the Barriers with Next-gen High-Performance Interconnect

Speaker:
Ashrut Ambastha, Senior Architect, Mellanox

We invite all participants and attendees for an open discussion on advancements in high-performance interconnect for HPC, storage and cloud-computing. In this session we will talk about networks ranging from the high-end HDR Infiniband interconnect for flagship systems to virtualized clouds that can run HPC workloads as efficiently as bare-metal hardware. We will also talk upon emerging standards in high-performance flash based storage systems and how technologies like NVMe over fabrics is breaking the traditional storage bottlenecks. We will also cover user wish-lists and needs for future HPC implementations and would be happy to take it as a feature request for our subsequent offerings.

Day 3 – Wednesday, December 21

Breakfast @ 7:30, Breaks @ 9:30 and 3:00, Lunch @ 12:00 (1 hour)

8:30 AM – 9:30 AM Wednesday, December 21

HiPC 2016 Keynote Presentation 2
Session Chair: Viktor Prasanna

China's HPC development in the next 5 years
Depei Qian
Sun Yat-sen University and Beihang University, China

Abstract: After a brief review of HPC research and development in China's high-tech R&D program, this talk will introduce the plan of HPC development under the new Key R&D Program of China in the thirteenth 5-year plan. The major challenges in establishing the eco-system for high performance computing in China will be discussed, including the technical issues in developing the next generation high performance computers, the need for developing system/application software for the systems based on domestically developed processors, and the mechanism for establishing a sustainable national HPC environment. The goal and the major activities of the new key project on HPC will be presented.

10:00 AM – 12:00 PM Wednesday, December 21

Technical Session 4: Numerical applications
Session Chair: Ajay Gupta

Balancing locality and concurrency: solving sparse triangular systems on GPUs
Andrea Picciau, Gordon E. Inggs, John Wickerson, Eric C. Kerrigan and George Constantinides (Imperial College UK, United Kingdom)

Tensor Contractions with Extended BLAS Kernels on CPU and GPU
Yang Shi, U.N. Niranjan and Animashree Anandkumar (University of California, Irvine, USA); Cris Cecka (NVIDIA Research, USA)

High performance Horizontal Diffusion Calculations in Ocean Models on Intel® Xeon Phi™ Coprocessor Systems
Aketh TM, Sathish Vadhiyar, PN Vinayachandran, and Ravi Nanjundiah (Indian Institute of Science, Bangalore, India)

Memory-Efficient Parallel Simulation of Electron Beam Dynamics Using GPUs
Kamesh Arumugam, Alexander Godunov, Desh Ranjan, Balsa Terzić and Mohammad Zubair (Old Dominion University, USA)

Cache-friendly Design for Complex Spatially-variable Coefficient Stencils on Many-core Architectures
Jiarui Fang, Haohuan Fu and Guangwen Yang (Tsinghua University, P.R. China)

10:00 AM – 12:00 PM Wednesday, December 21

IRUS 2: Advances in Applied Machine Learning and Analytics

Gokul Swamy, Amazon
Topic: Machine Learning for the E-Commerce Sector

Ramakrishna Urs, Infosys
Topic: Applied Machine Learning for automated workflow management and account classifications

Joy Mustafi, Microsoft
Topic: Applications of Cognitive Computing

1:00 PM – 3:00 PM Wednesday, December 21

Technical Session 5: Resilience and compilers
Session Chair: Ponnuswamy Sadayappan

Using Message Logs and Resource Use Data for Cluster Failure Diagnosis
Edward Chuah (The Alan Turing Institute and University of Warwick, U.K., and Singapore Polytechnic, Singapore); Arshad Jhumka (University of Warwick, United Kingdom); James C. Browne (UT Austin, USA); Nentawe Gurumdimma (University of Jos, Nigeria and University of Warwick, United Kingdom); Sai Narasimhamurthy (Seagate Technology, United Kingdom); Bill Barth (The University of Texas at Austin, USA)

A Low-Cost Multi-Failure Resilient Replication Scheme for High Data Availability in Cloud Storage
Jinwei Liu and Haiying Shen (Clemson University, USA)

PRESAGE: Protecting Structured Address Generation against Soft Errors
Vishal Sharma and Ganesh Gopalakrishnan (University of Utah, USA); Sriram Krishnamoorthy (Pacific Northwest National Laboratory, USA)

MP-Index: A Multi-Predicate Publish/Subscribe Mechanism for Internet of Things
Satvik Patel (Parul University, India); Sunil Jardosh (Progress Software, India); Ashwin Makwana (CHARUSAT University, India)

Phase Directed Compiler Optimizations
Era Jain (IIT Kanpur (Now at Google), USA); Subhajit Roy (Indian Institute of Technology, Kanpur, India)

Automatic Code Generation for Iterative Multi-dimensional Stencil Computations
Mariem Saied and Jens Gustedt (INRIA and ICube Université de Strasbourg, France); Gilles Muller (INRIA and LIP6 – Sorbonne Universités, CNRS, UPMC, France)

3:30 PM – 5:30 PM Wednesday, December 21

Student Research Symposium (SRS)
Dedicated Poster Session: Student authors available at posters

Starting 6:30 PM Wednesday, December 21

- **Presentation of Awards**
- **Cultural Event: Hindustani Classical Ensemble (details available at event)**
- **Followed by HiPC 2016 Banquet (featuring Hyderabadi cuisine, aka Deccan cuisine.)**

Day 4 – Thursday, December 22

Breakfast @ 7:30, Break@ 9:30, Lunch @ 12:00

8:30 AM – 9:30 AM Thursday, December 22

HiPC 2016 Keynote Presentation 3
Session Chair: Ramamurthy Badrinath

Toward Extreme-Scale Processor Chips
Josep Torrellas
University of Illinois Urbana-Champaign, USA

Abstract: As transistor sizes continue to scale, we are about to witness stunning levels of chip integration, with 1,000 cores on a single die, and increasing levels of die stacking. Transistors may not be much faster, but there will be many more of them. In these architectures, efficient communication and synchronization will be a challenge. Moreover, energy and power will constrain the designs even more than they do today. In this context, this talk presents some of the technologies that we may need to deploy to exploit these architectures. To enable data sharing, we need novel synchronization and fence hardware. For low-latency communication, we may leverage on-chip wireless networks. Cores need to be voltage scalable, i.e., flexibly operate both at high and low voltage ranges. Techniques for efficient energy use need to be widespread. Finally, hardware extensions to ease programming will provide a competitive edge. A combination of all of these techniques -- and more-- are needed.

10:00 AM – 12:00 PM Thursday, December 22

Technical Session 6:
Parallel algorithms: Data structures, resource allocation, and linear algebra
Session Chair: Neelima Bayyapu

Fast Parallel Operations on Search Trees
Yaroslav Akhremtsev and Peter Sanders (Karlsruhe Institute of Technology, Germany)

Efficient Parallel Ear Decomposition of Graphs with Application to Betweenness-Centrality
Charudatt Pachorkar, Meher Chaitanya, and Kishore Kothapalli (International Institute of Information Technology, Hyderabad, India); Debajyoti Bera (Indraprastha Institute of Information Technology, Delhi, India)

Parallelization of Bin Packing on Multicore Systems
Sayan Ghosh and Assefaw H. Gebremedhin (Washington State University, USA)

Scheduling of Linear Algebra Kernels on Multiple Heterogeneous Resources
Olivier Beaumont, Terry Cojean, Lionel Eyraud-Dubois, Abdou Guermouche, and Suraj Kumar (INRIA Bordeaux Sud-Ouest and University of Bordeaux, France)

An Alternative Approach of the SPIKE Preconditioner for Finite Element Analysis
Leonardo Muniz de Lima, and Brenno Albino Lugon and Lucia Catabriga (Universidade Federal do Espírito Santo, Brazil)

CMT-bone - A Proxy Application for Compressible Multiphase Turbulent Flows
Tania Banerjee, Jason Hackl and Mrugesh Shringarpure (University of Florida, USA); Tanzima Islam (Lawrence Livermore National Laboratory, USA); S. Balachandar, Thomas Jackson and Sanjay Ranka (University of Florida, USA)

1:30 PM – 3:30 PM Thursday, December 22

Technical Session 7: Software architecture

Session Chair: Yogesh Simmhan

Compiler Support for Software Cache Coherence
Sanket Tavarageri (The Ohio State University, USA); Wooil Kim and Josep Torrellas (University of Illinois at Urbana-Champaign, USA); P Sadayappan (The Ohio State University, USA)

Predictive Evaluation of Partitioning Algorithms Through Runtime Modelling
Richard A. Bunt, Stephen A. Wright and Stephen A. Jarvis (University of Warwick, United Kingdom); Yoon K. Ho and Matthew J. Street (Rolls-Royce, United Kingdom)

Performance Prediction of Parallel Applications Based on Small-Scale Executions
Rodrigo Escobar and Rajendra V. Boppana (University of Texas at San Antonio, USA)

ERICO: Effective Removal of Inline Caching Overhead in Dynamic Typed Languages
Gem Dot (Universitat Politècnica de Catalunya, Spain); Alejandro Martínez (ARM, United Kingdom); Antonio González (Universitat Politècnica de Catalunya, Spain)

A Directory Cache with Dynamic Private-Shared Partitioning
Joan Valls and María Engracia Gómez (Universidad Politecnica de Valencia, Spain); Alberto Ros (University of Murcia, Spain); Julio Sahuquillo (Universidad Politecnica de Valencia, Spain)

Steal-A-GC: Framework to Trigger GC during Idle Periods in Distributed Systems
Sujoy Saraswati, Soumitra Chatterjee and Ranganath Ramachandra (HPE, India)

2017

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Jaipur, India